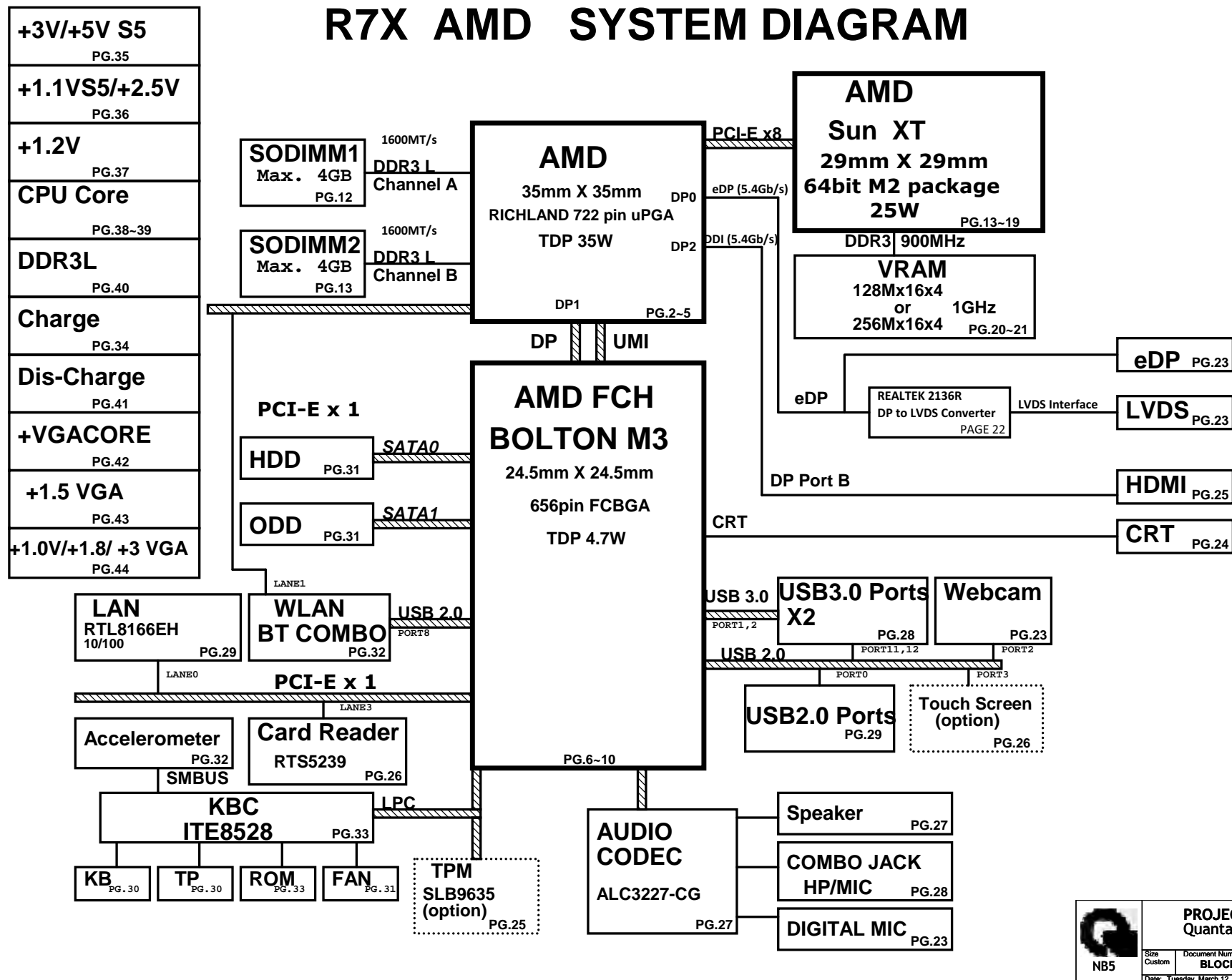


R7X AMD SYSTEM DIAGRAM

01

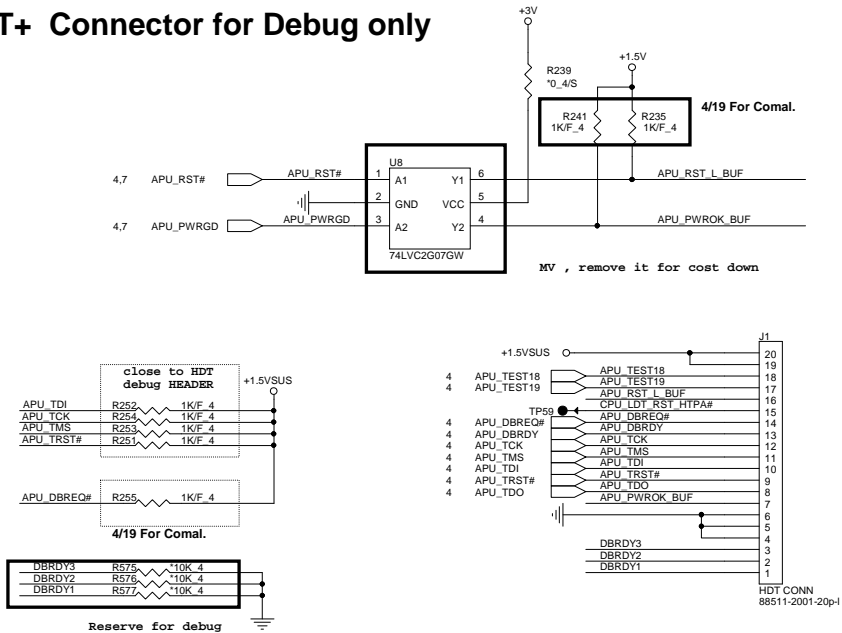


PROJECT : R7X
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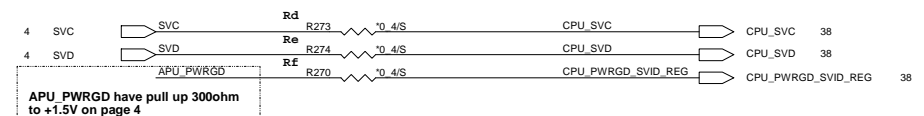
Size Custom	Document Number BLOCK DIAGRAM	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 1 of 43	



VID Override Circuit

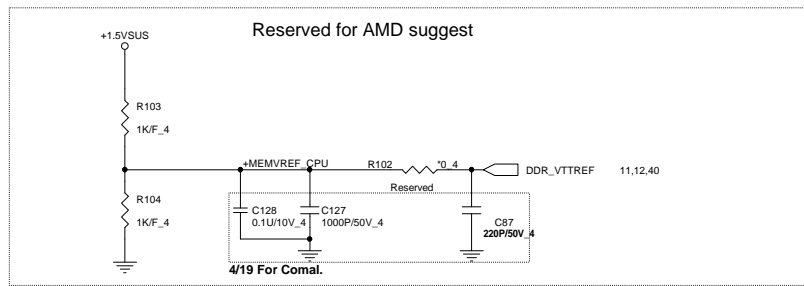
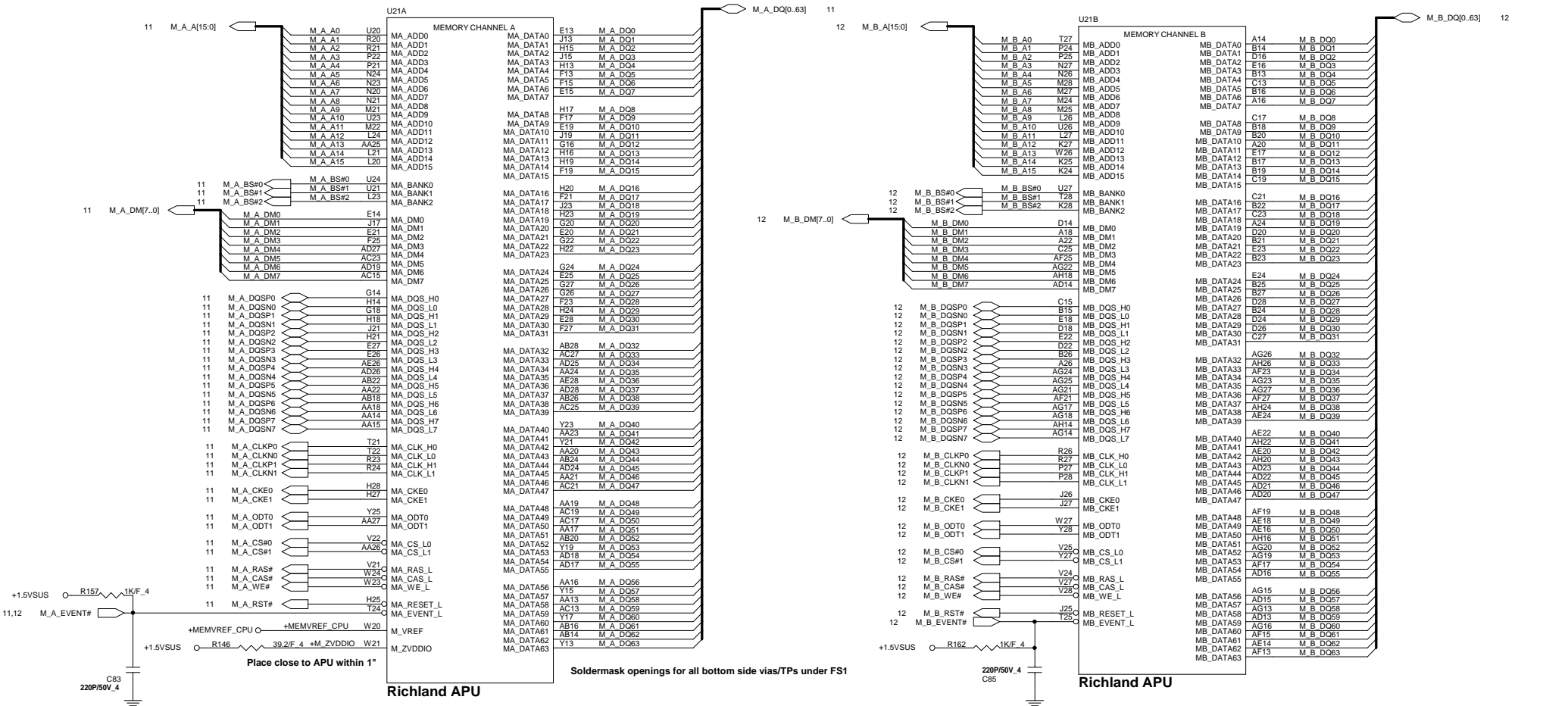


		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



PROJECT : R7X
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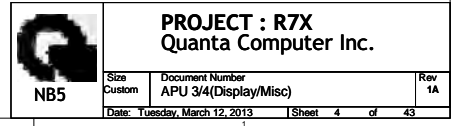
Size Custom	Document Number APU 1/4(PCIE/UMI/GPP/HDT)	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 2 of 43	



+3V5S 4,6,8,9,10,25,32,33,35,36,38,41,43
+1.5VSUS 2,4,5,11,12,40,41,43

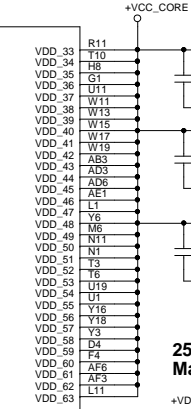
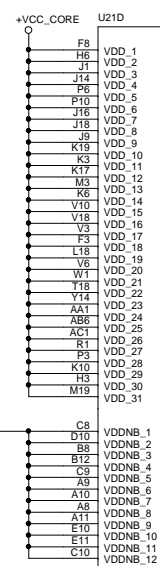
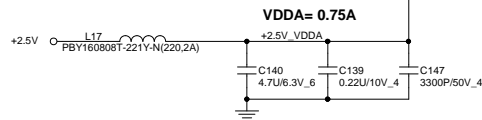
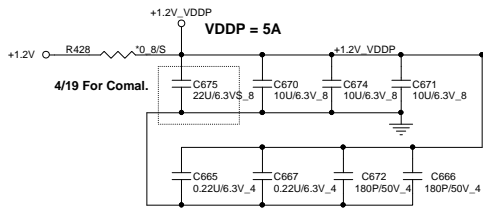
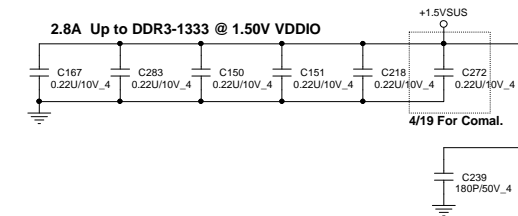
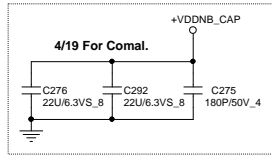
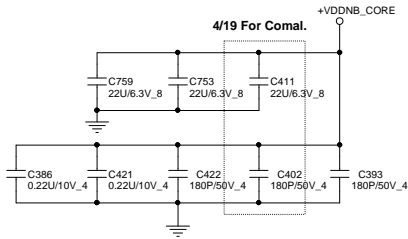
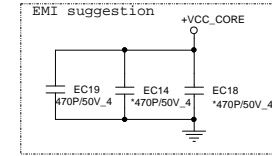
PROJECT : R7X
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Size Custom	Document Number APU 2/4(DDR3 MEM I/F)	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 3	of 43



APU POWER TABLE

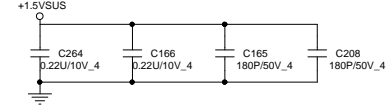
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



36A Maximum IDDspike 50A

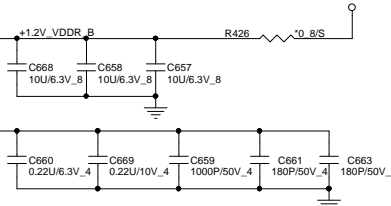
25A Maximum IDDNBspike 33A

DECOUPLING between PROCESSOR and DIMMs Across VDDIO and VSS split



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

VDDR = 3.3A (Up to DDR3-1333 @ 1.5V)



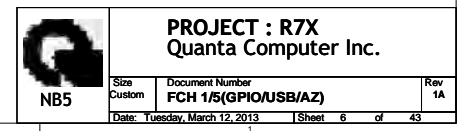
Richland APU

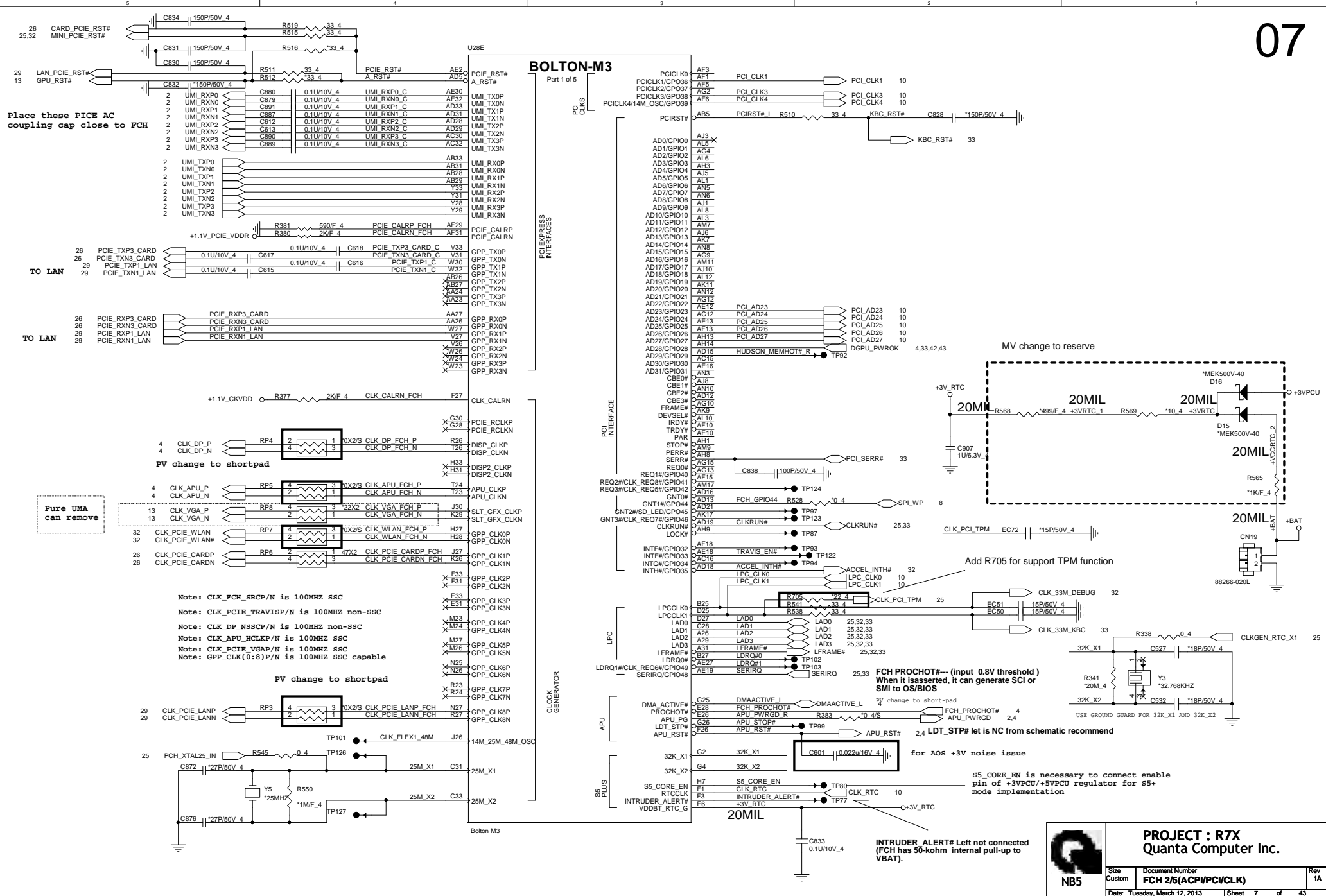
Richland APU

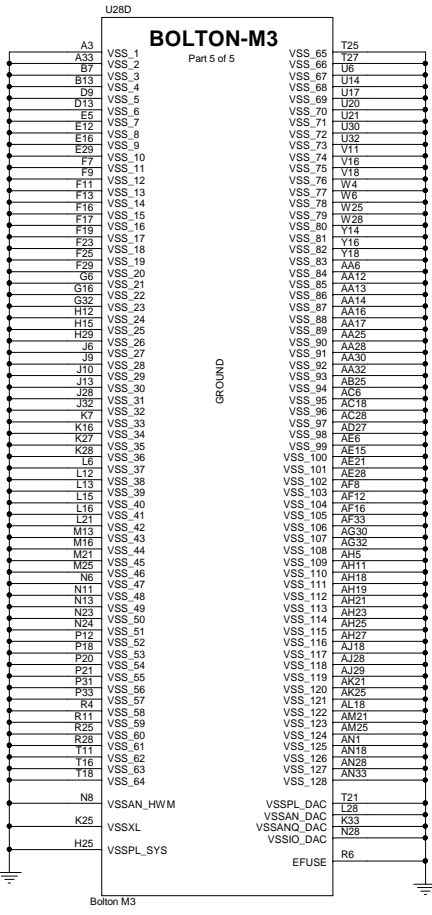


PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number APU 4/4(Power/GND)	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 5 of 43	







ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	DIS		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

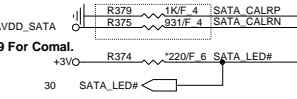
GPIO52 internal pull Hi 8.2K to +3V
 GPIO53 internal pull Hi 8.2K to +3V
 GPIO54 internal pull Hi 8.2K to +3V
 GPIO57 internal pull Hi 8.2K to +3V
 GPIO58 internal pull Hi 8.2K to +3V

PLACE SATA AC COUPLING CAPS CLOSE TO HUDSON-M2/M3

SATA HDD

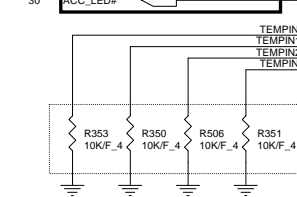
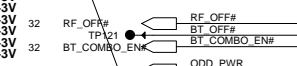
SATA ODD

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3



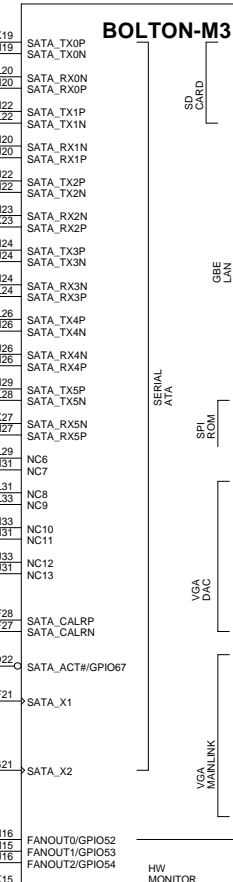
4/19 For Comal.
 +3V0
 R374 *220F 6
 SATA_LED#
 AD22
 SATA_ACT#/GPIO67
 AF21
 SATA_X1
 AG21
 SATA_X2

Integrated Clock Mode: Leave unconnected.



SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no support side port

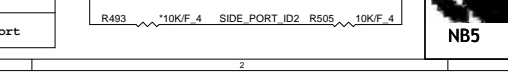
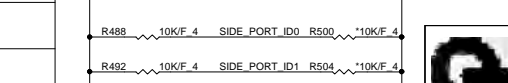
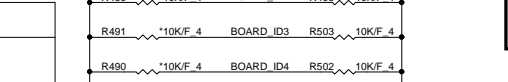
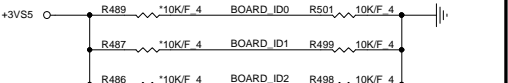
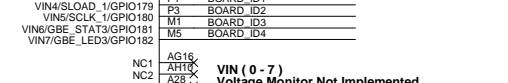
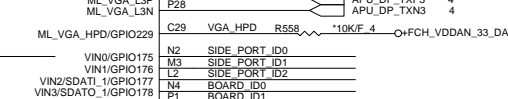
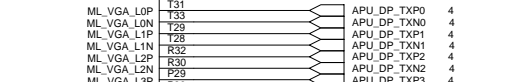
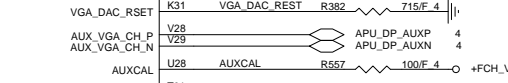
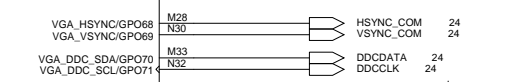
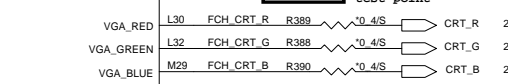
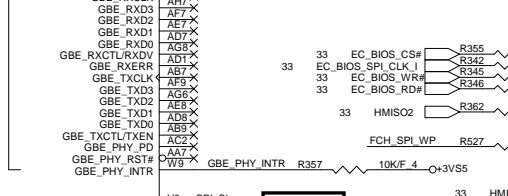
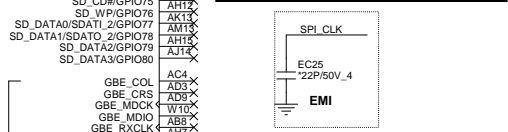
BOLTON-M3 Part 2 of 5



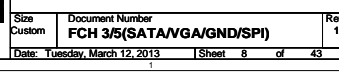
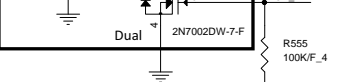
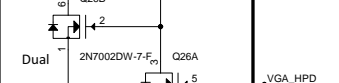
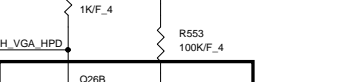
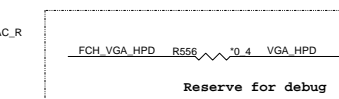
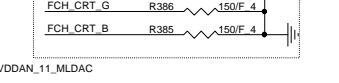
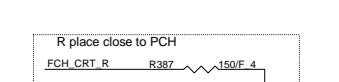
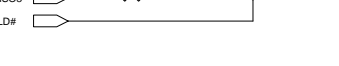
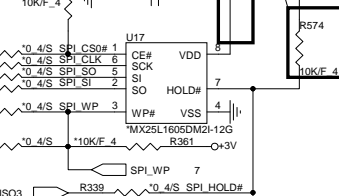
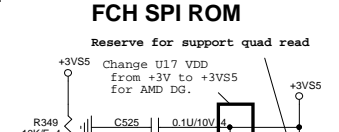
TEMP (0 - 3)
 Temp Monitor Not Implemented
 10-KΩ 5% pull-up to +3V5
 or 10-KΩ 5% pull-down

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no support side port

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023



Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

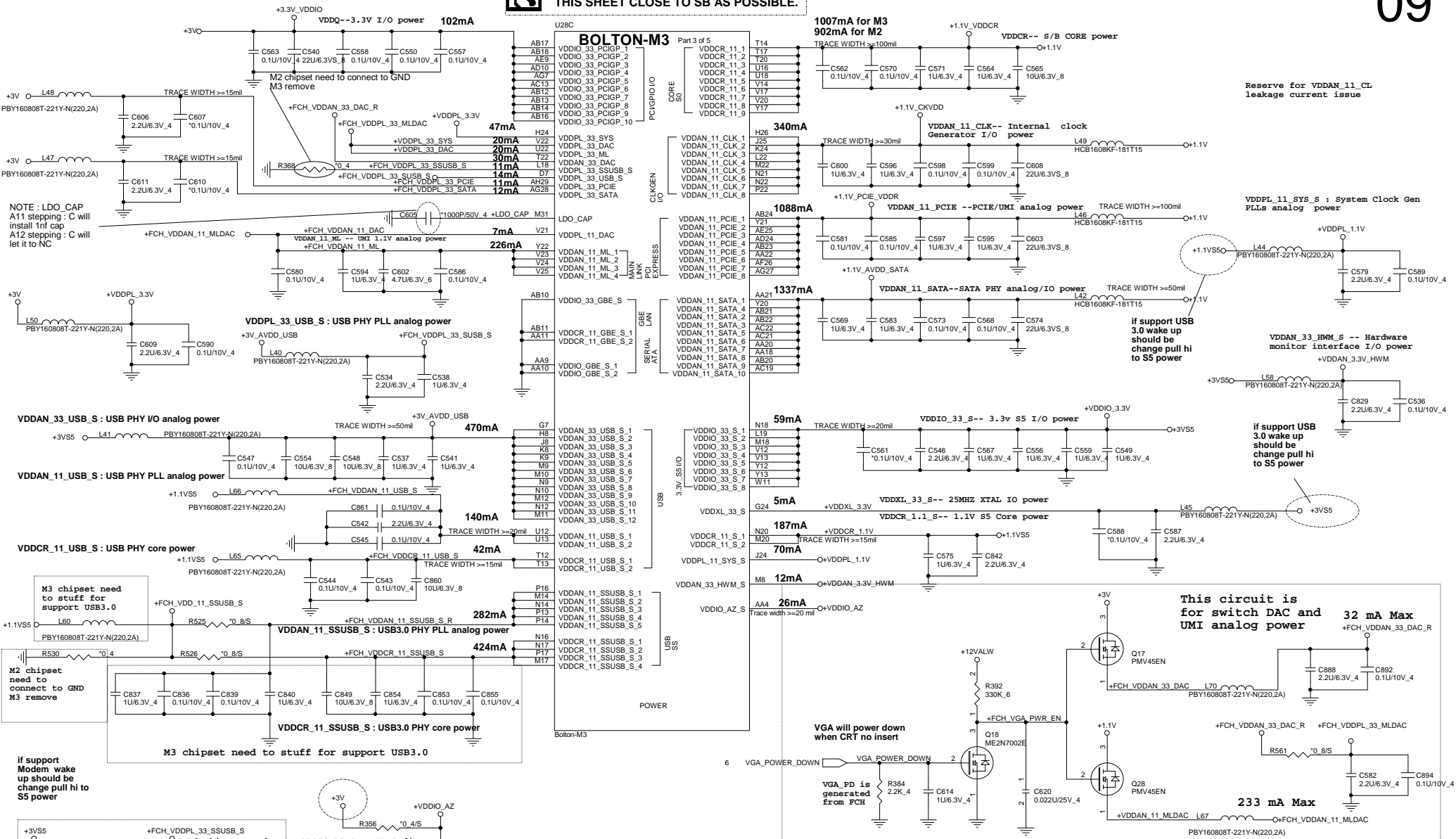


SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no support side port

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no support side port



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



This circuit is for switch DAC and UMI analog power

32 mA Max

FCH_VDDAN_33_DAC_R

FCH_VDDPL_33_MLDC

233 mA Max

FCH_VDDAN_11_MLDC

FCH_VDDAN_11_MLDC

FCH_VDDAN_11_MLDC

FCH_VDDAN_11_MLDC

FCH_VDDAN_11_MLDC



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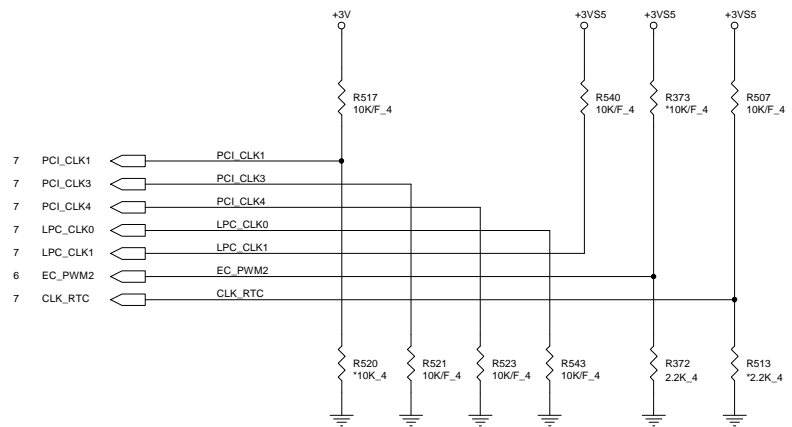
Size Custom Document Number FCH 4/5(POWER)

Date: Tuesday, March 12, 2013 Sheet 9 of 43

Rev 1A

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

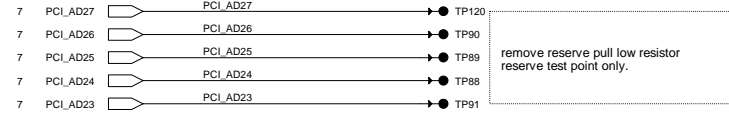


REQUIRED STRAPS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	ALLOW PCIe Gen2 DEFAULT	USE DEBUG STRAP	non-Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIe Gen1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

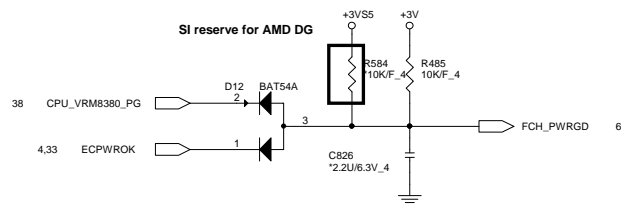
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



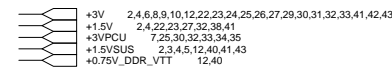
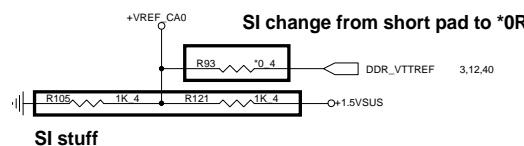
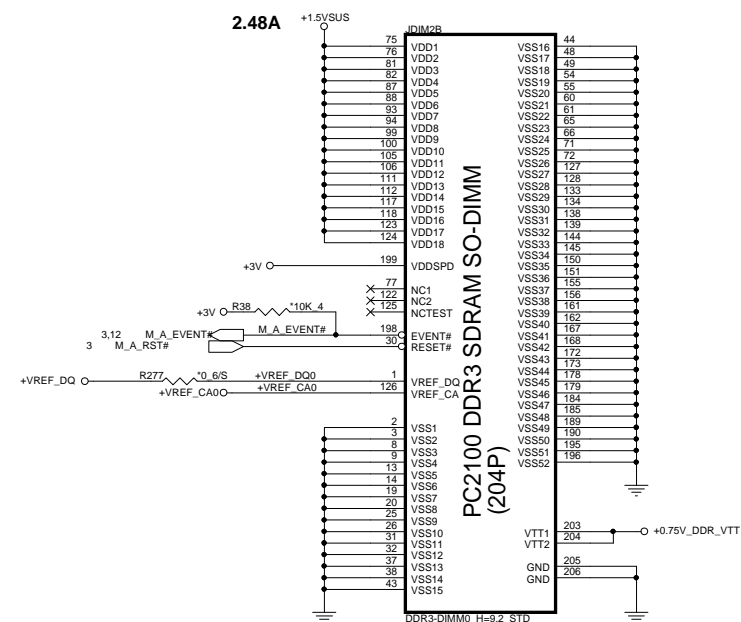
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

FCH_PWRGD

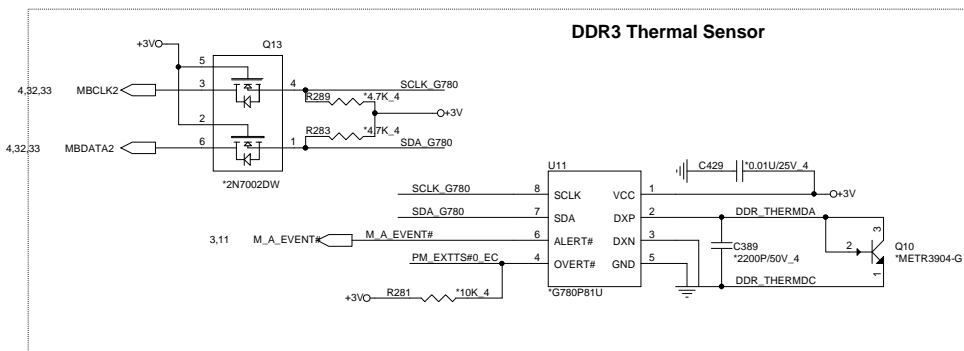
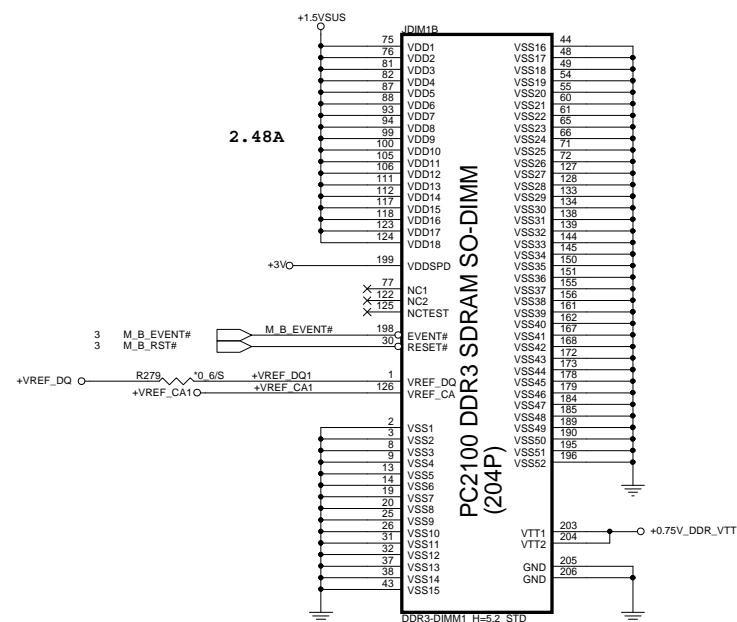


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Size Custom	Document Number FCH 5/5(Strap &PWRGD)	Rev 1A
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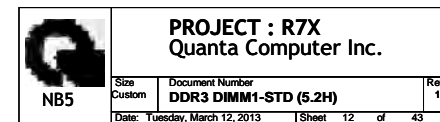
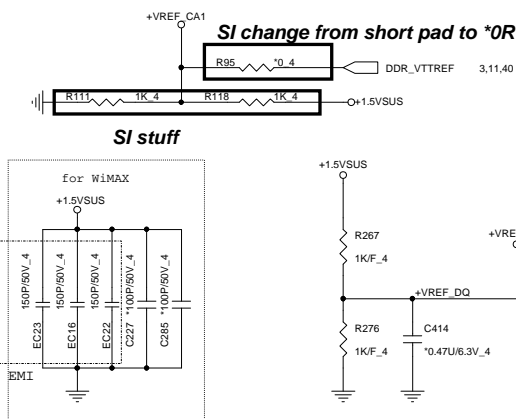
The schematic diagram illustrates the power supply section of the reference design, showing four main power rails and their connections to various components:

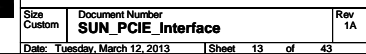
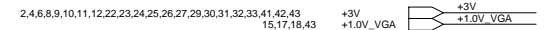
- +1.5V_SUS:** Connected to pins C129, C134, C157, C219, C244, C265, C259, C206, C216, C88, C263, EC11, EC9, EC13, and EC10. A dashed box labeled EMI indicates a common mode choke connected to the +1.5V_SUS and +3V rails.
- +0.75V_DDR_VTT:** Connected to pins C46, C45, C52, C44, C43, C34, C47, C54, and C53.
- +3V:** Connected to pins C61, C62, and C60.
- +VREF_DQ1:** Connected to pins C424 and C423.
- +VREF_CA1:** Connected to pins C116, C122, and C118.

Decoupling capacitors and their values are specified for each rail:

- +1.5V_SUS:** C129, C134, C157, C219, C244, C265, C259, C206, C216, C88, C263, EC11, EC9, EC13, EC10.
- +0.75V_DDR_VTT:** C46, C45, C52, C44, C43, C34, C47, C54, C53.
- +3V:** C61, C62, C60.
- +VREF_DQ1:** C424, C423.
- +VREF_CA1:** C116, C122, C118.

The diagram also shows various decoupling capacitors and their values, such as 100uF/6.3V/6, 1uF/6.3V/4, 0.1uF/10V/4, 1000pF/50V/4, and 0.047uF/10V/4.





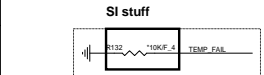
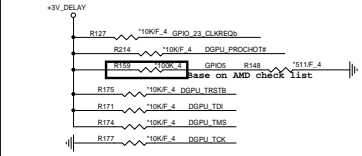
PS1 BIT3->BIT1 (3-bit)	Vendor	Vendor P/N	QCI P/N (TOP B/S)
011	Hynix	128Mx16 *4 B5TC2G63PFR-11C	AKDSM2DTW02
100	Micron	128Mx16 *4 MT41J128M16JT-093G:K	AKDSMGSTL16
101	Samsung	128Mx16 *4 K4W2G1646B-BC1A	AKDSMGST534

Only for Test			
PS1 BIT3->BIT1 (3-bit)	Vendor	Vendor P/N	QCI P/N
000	Hynix	256Mx16 *4 B5TC4G63AFR-11C	AKDSPGWTW07
001	Micron	256Mx16 *4 MT41J256M16HA-093G:E	AKDSPSTL100
010	Samsung	256Mx16 *4 K4W4G1646B-HC1A	AKDSPST2T500

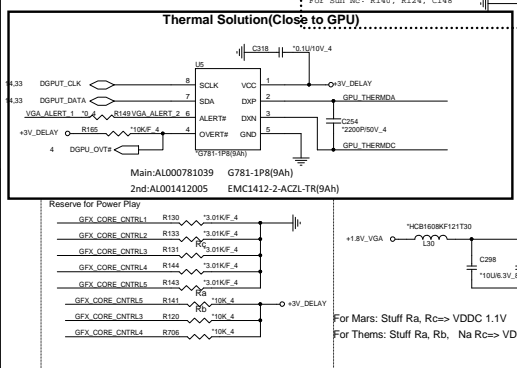
Samsung 2GB VRAM	ANDPG0T595	64W0V1646B-BC1A
Samsung 4GB VRAM	ANDPG2T501	64W0V1646B-HC1A
Hynix 2GB VRAM	ANDSG2T003	B5TC2G63PFR-11C
Hynix 4GB VRAM	ANDPGWT008	B5TC4G63AFR-11C
Micron 2G VRAM	ANDMGSTL17	MT41J128M16JT-093G:K
Micron 4G VRAM	AKDSPSTL01	MT41J256M16HA-093G:E

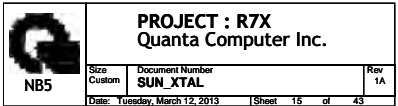
For Sun only :
AP10 / AV11 / AT11 / AR12 / AM12 / AU12 / AP12 : NC pin

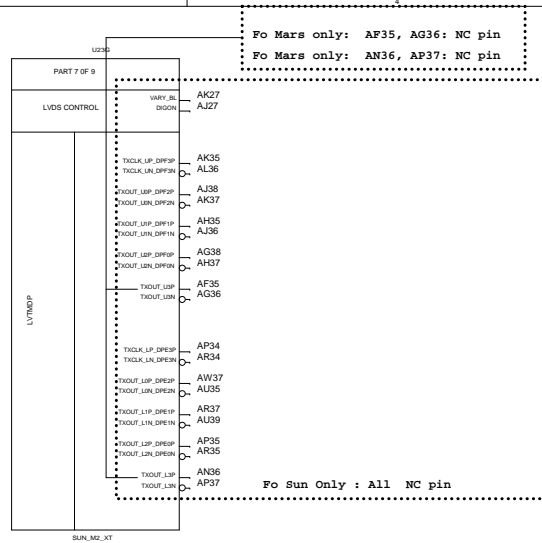
Access to SMBus and SDA/SCL is mandatory on all designs
Add test points on SMBus and SDA/SCL for debug



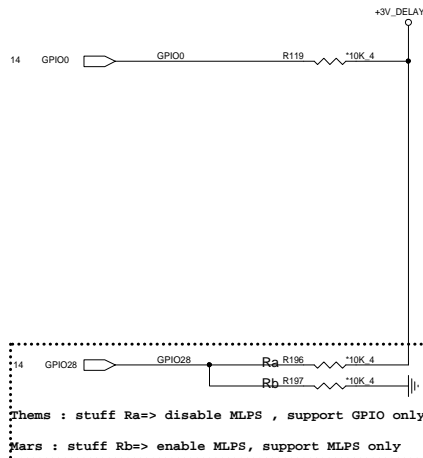
+3V_DELAY R150 10K 4 VGA_ALERT 1



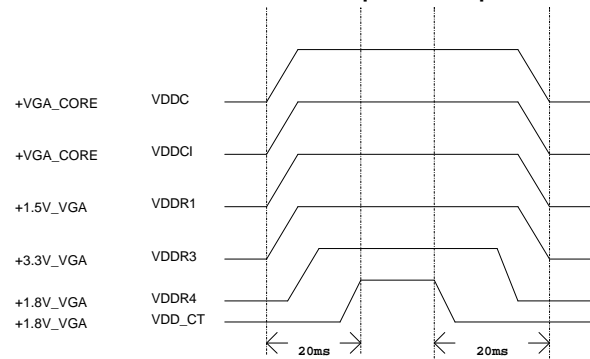




CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512kbit M25P05A (STD) 101 - 1Mbit M25P10A (STD) 101 - 4Mbit M25P40 (STD) 101 - 512kbit Fm25LV512 (Chingis) 101 - 1Mbit Fm25LV010 (Chingis)	001
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYN	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled Reserve for future ASIC	1
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE- ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	111



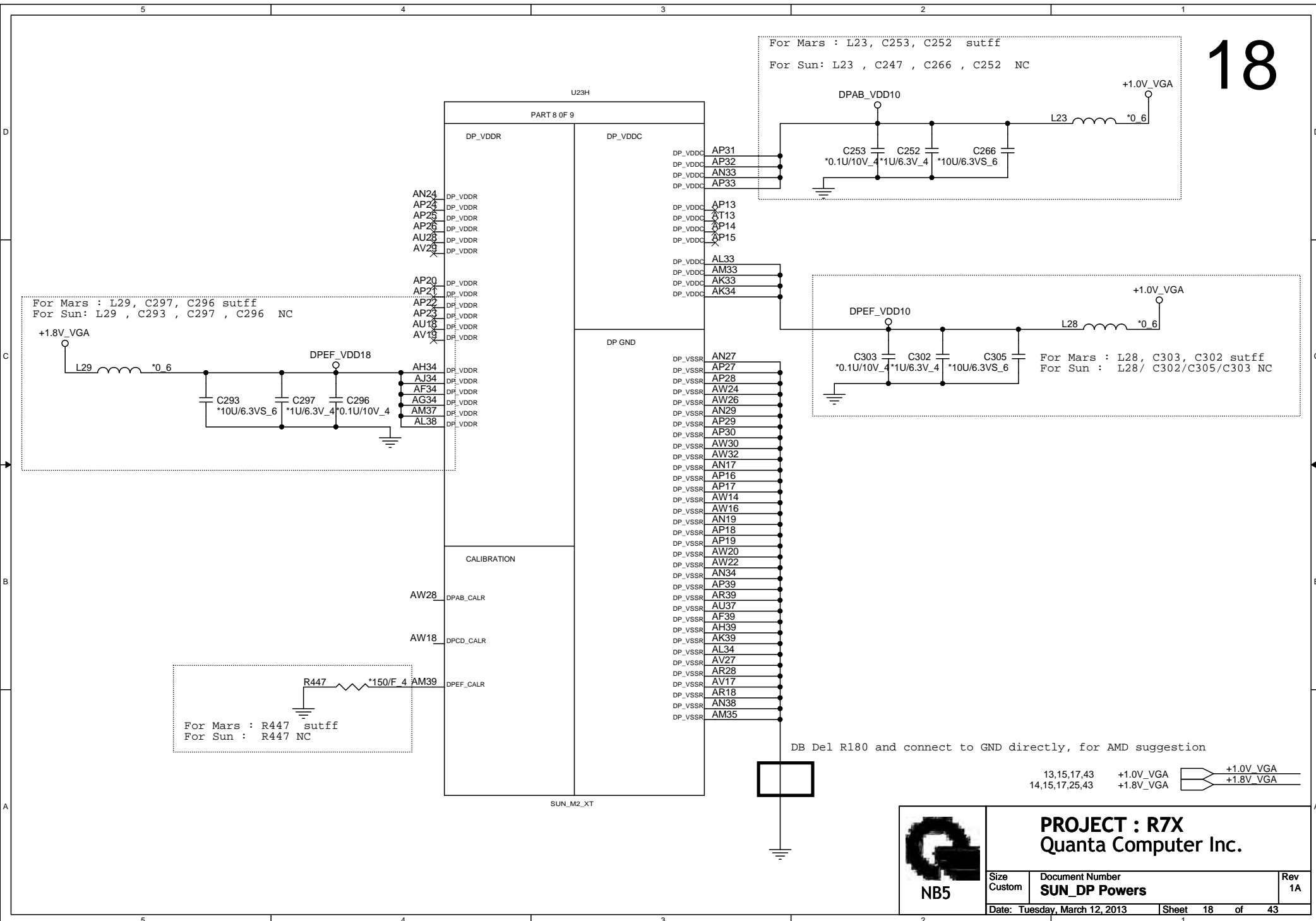
Power Up/Down Sequence



PROJECT : R7X
Quanta Computer Inc.

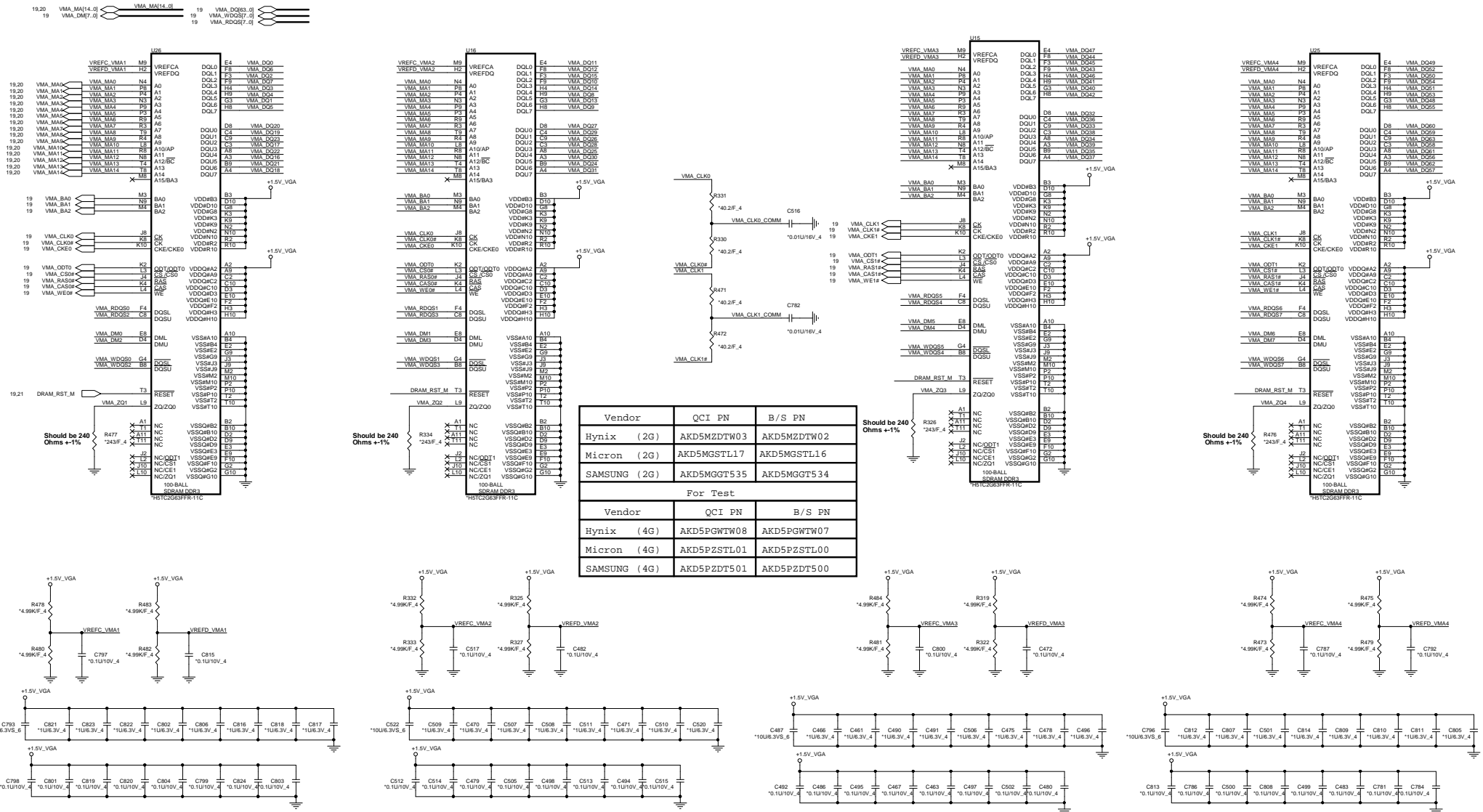
Size	Document Number	Rev
Custom	SUN_LVDS / STRAP	1A
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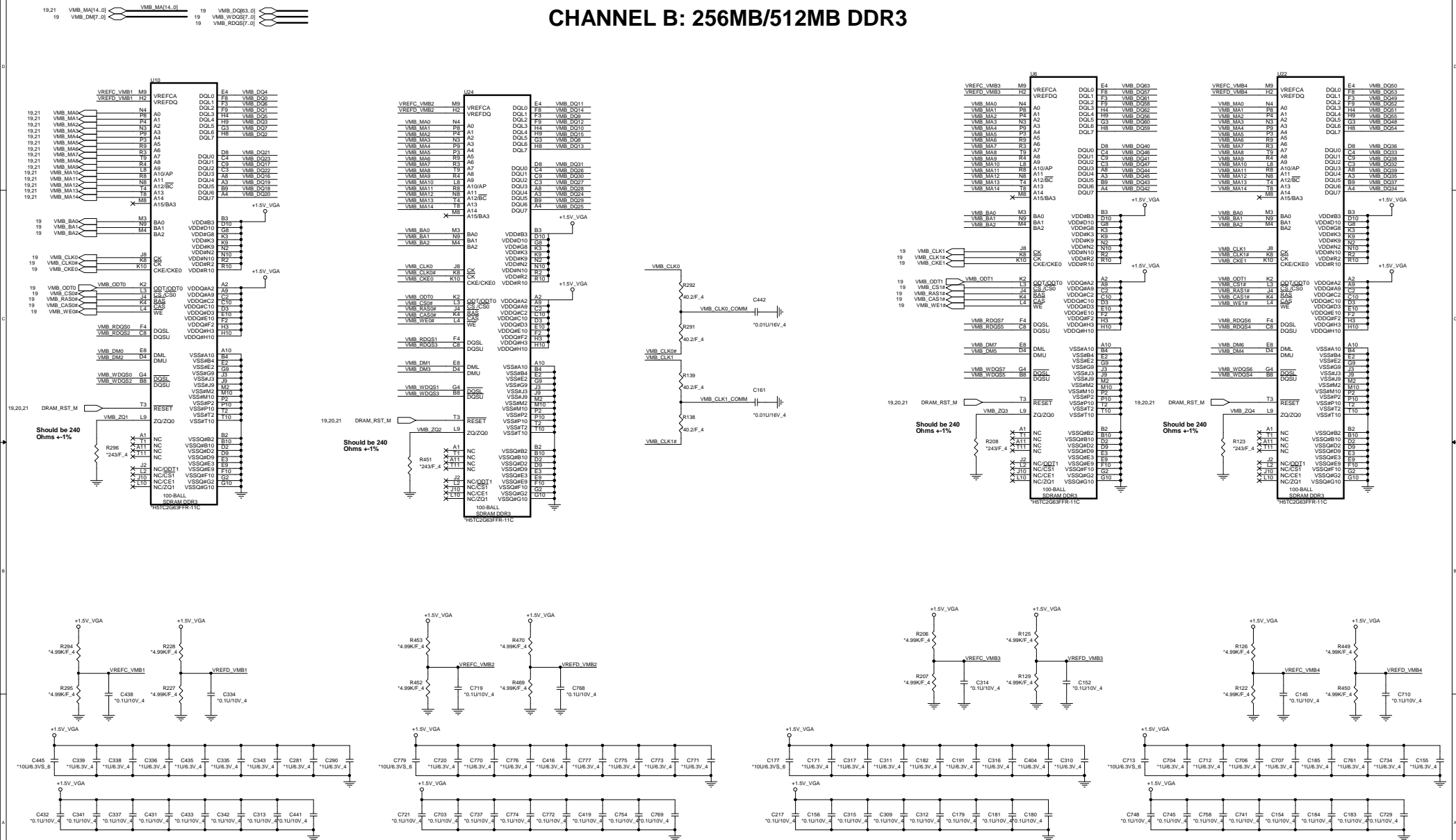


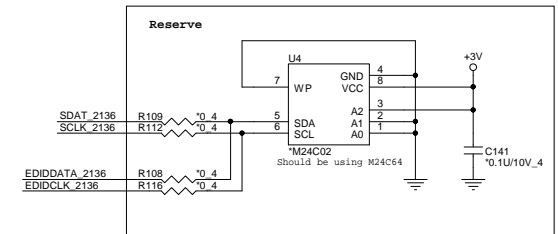
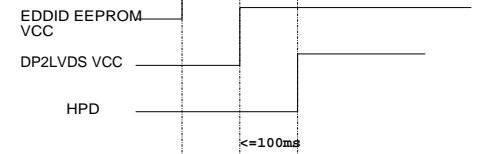


CHANNEL A: 256MB/512MB DDR3

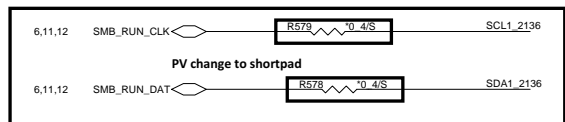


CHANNEL B: 256MB/512MB DDR3

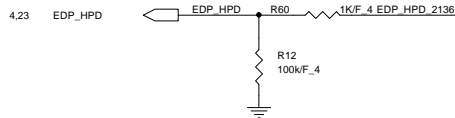




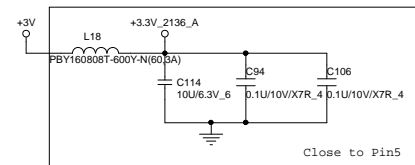
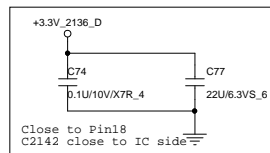
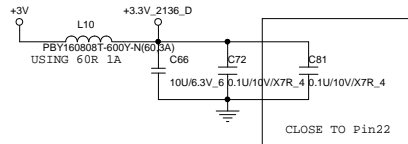
SMBUS



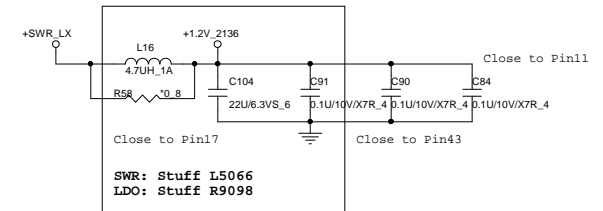
DB change from SMB_PCH_CLK/DAT to SMB_RUN_CLK/DAT



keep 80 Mile Trace

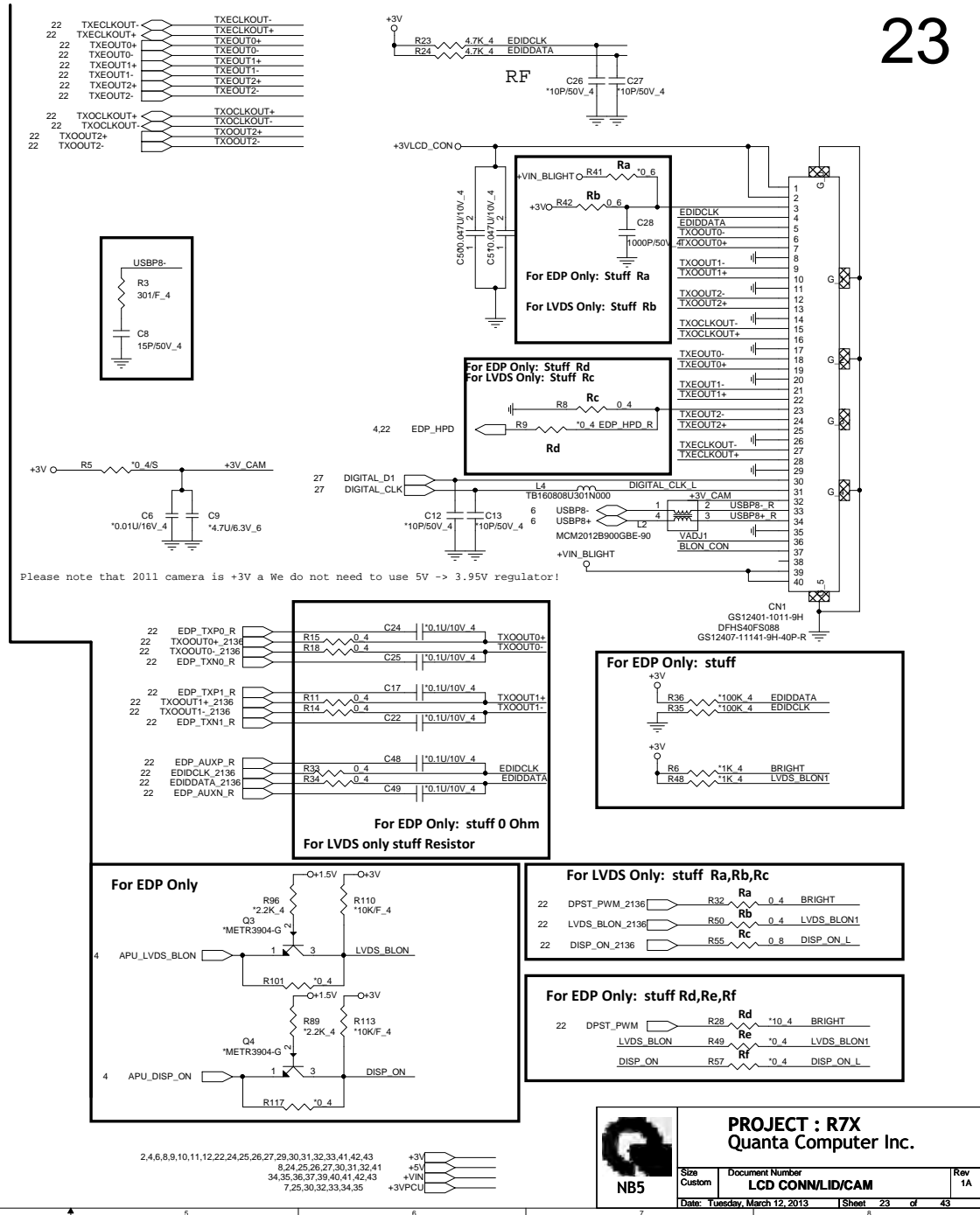


L69: need use CV-4709NM00 for Vendor suggestion

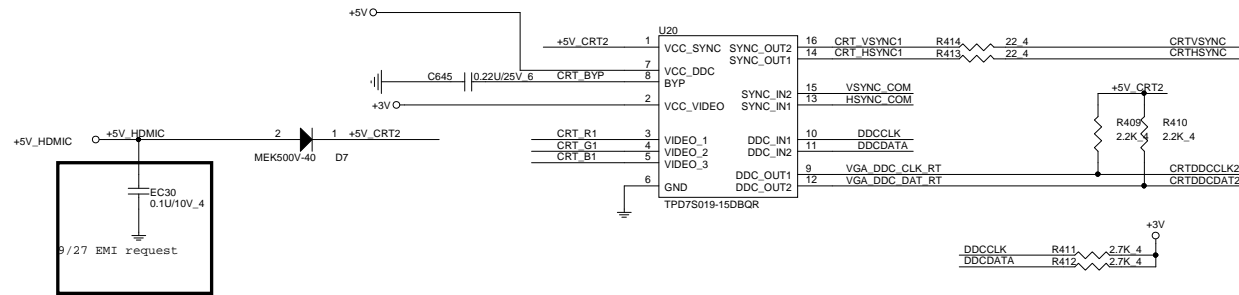
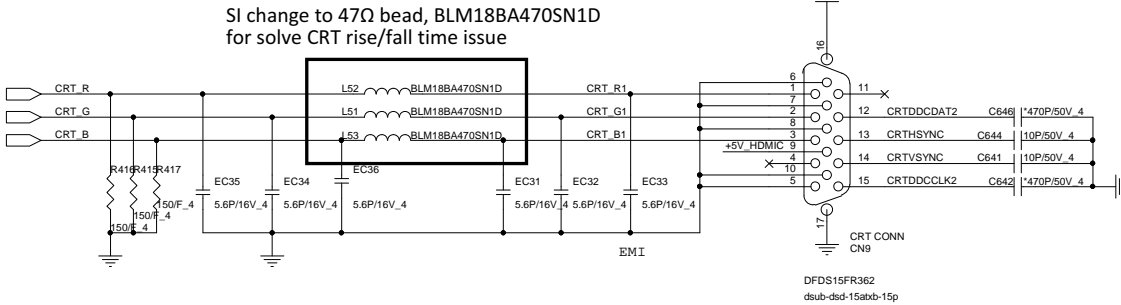


SWR: Stuff L5066
LDO: Stuff R9098

	PROJECT : R7X	
	Quanta Computer Inc.	
	Size Custom	Document Number LVDS converter RTD2136
Rev 1A	Date: Tuesday, March 12, 2013	Sheet 22 of 43



CRT PORT



HOLE

HOLE

FAN hole

PCH BKT

CPU BKT

VGA BKT

Nut PN:MBBU2005010

THERMAL BKT

KB lock

SI add

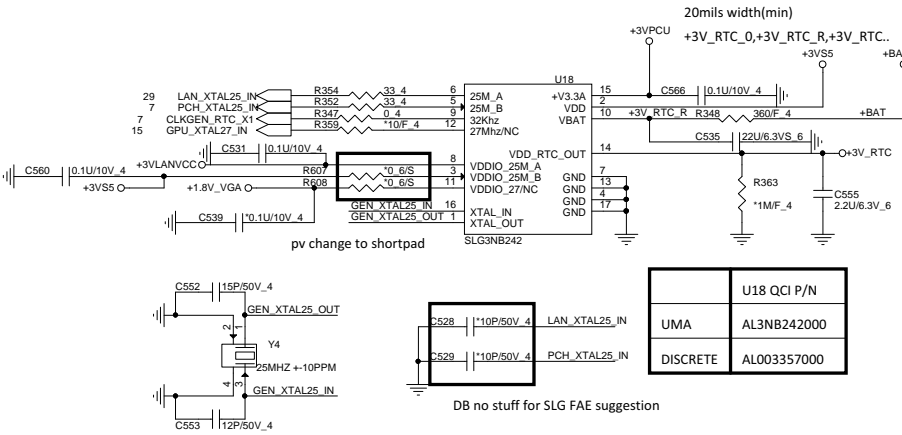
MV add



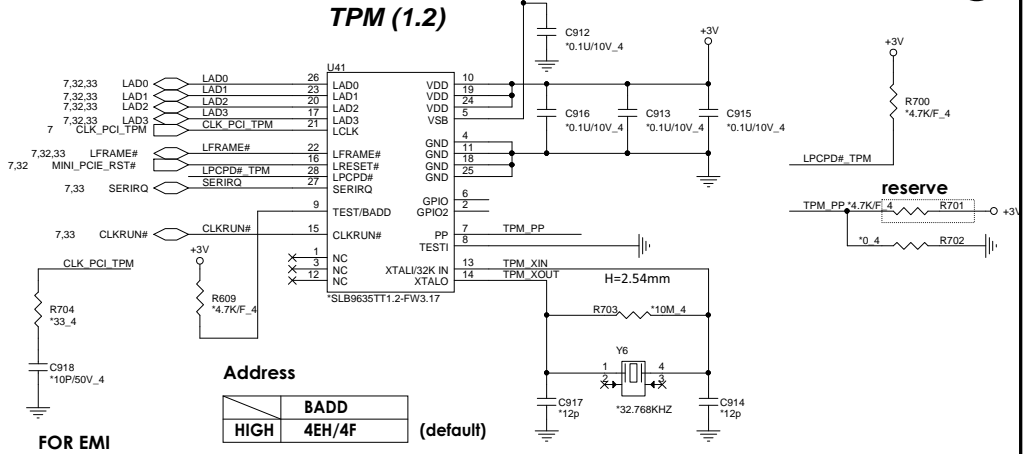
PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT_Hole	1A
Date:	Tuesday, March 12, 2013	Sheet 24 of 43

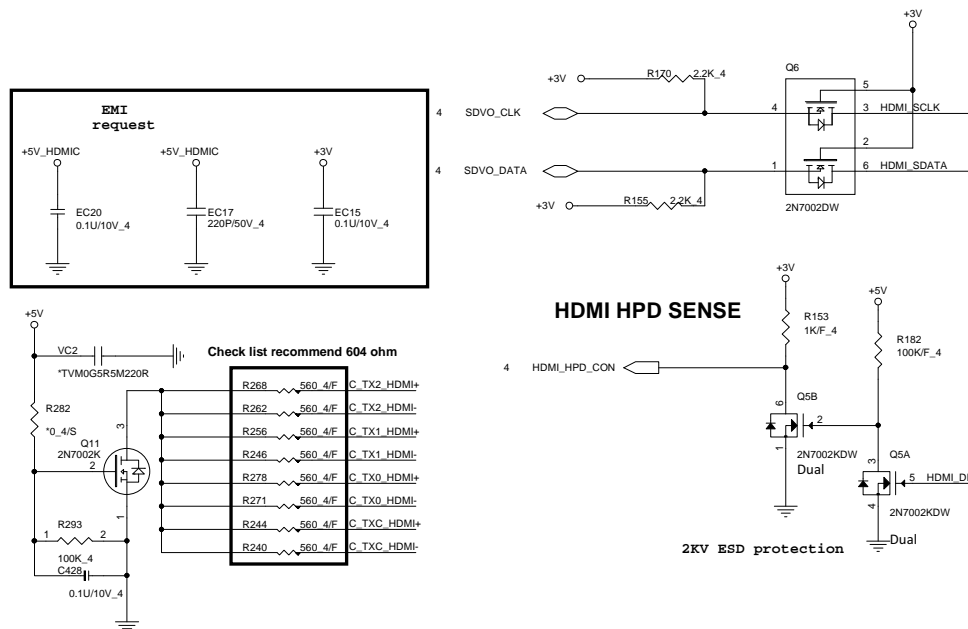
Green CLK Circuitry



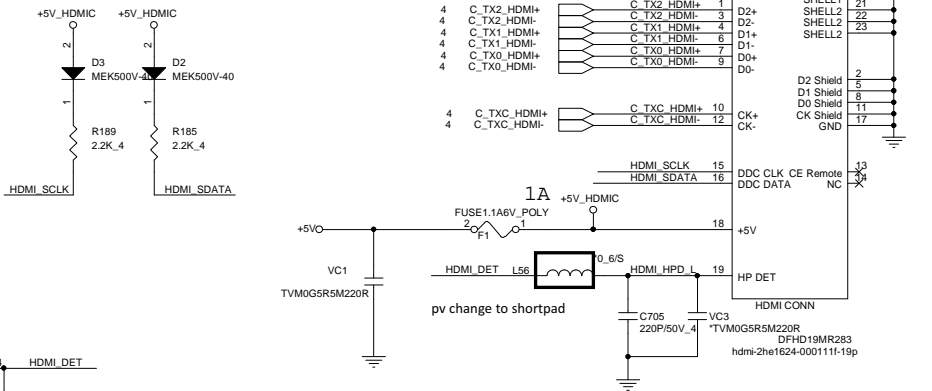
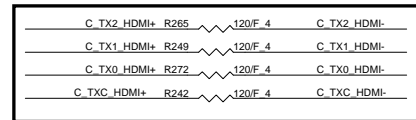
PV add



DISCRETE HDMI I2C SELECT Close to HDMI Connector

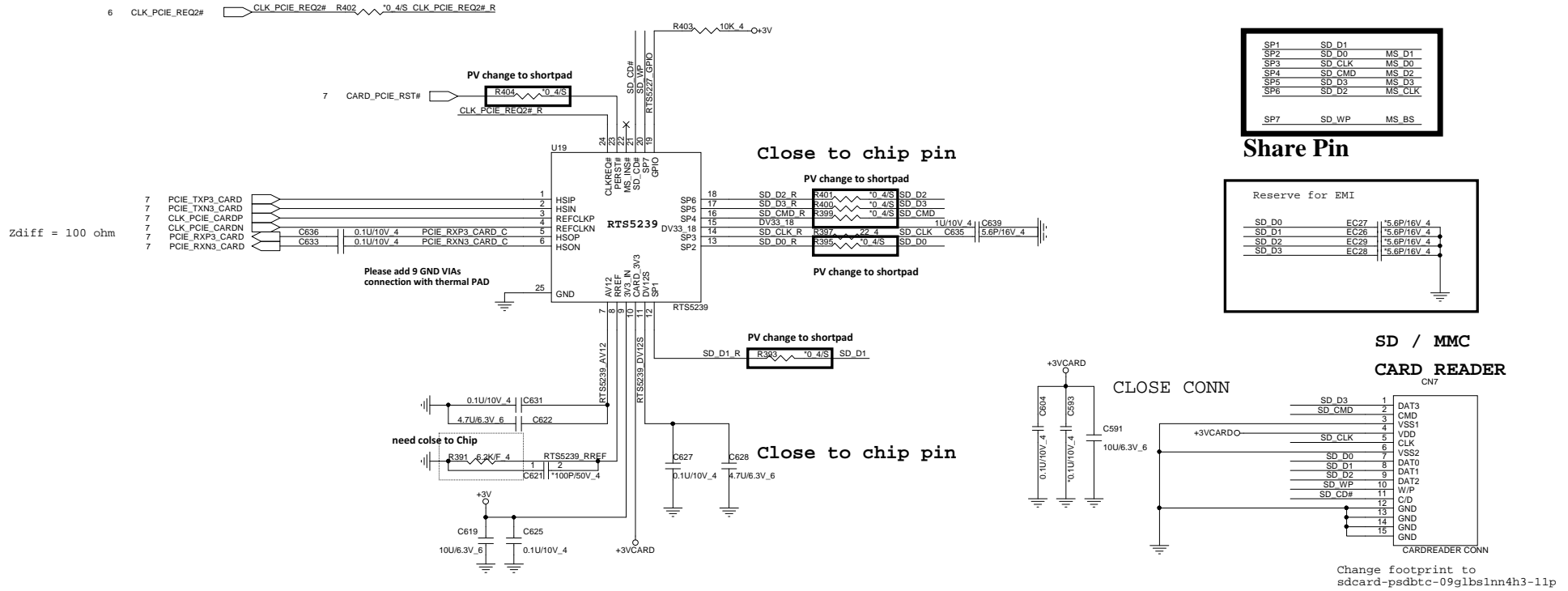


EMI request

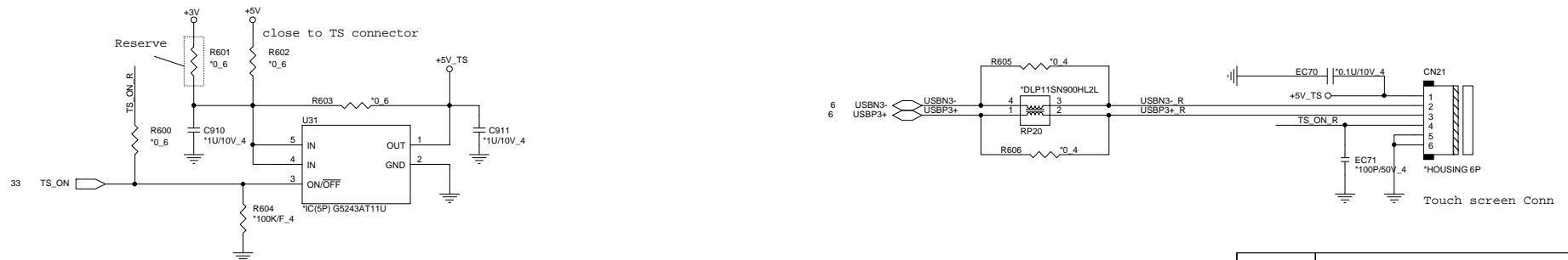


PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number HDMI	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 25 of 43	



Touch Screen Connector



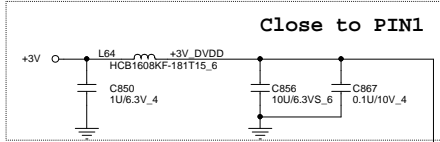
PROJECT : R7X
Quanta Computer Inc.

Size Custom Document Number
RTS5229 & CR SOCKET

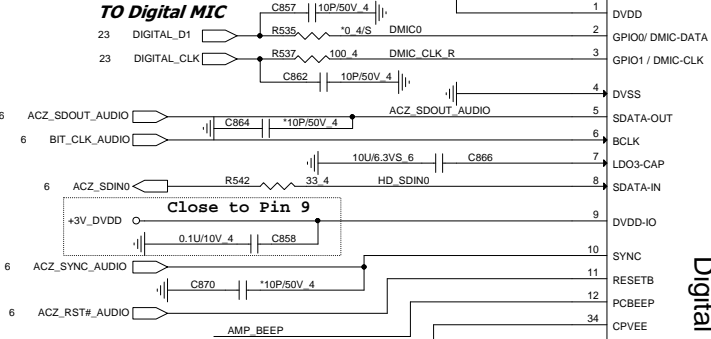
Date: Tuesday, March 12, 2013 Sheet 26 of 43

Rev 1A

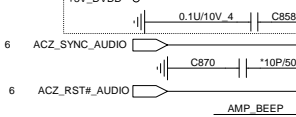
Close to PIN1



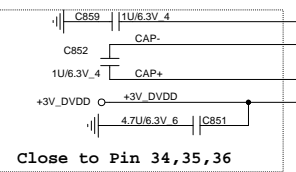
TO Digital MIC



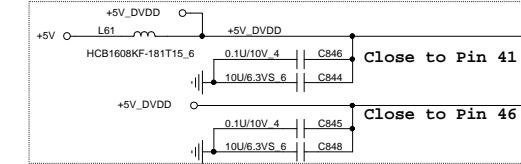
Close to Pin 9



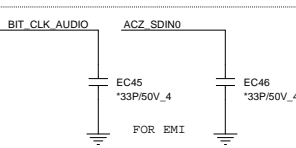
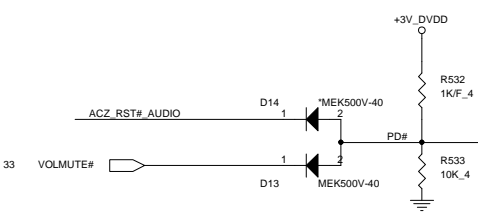
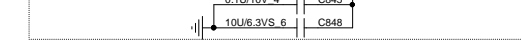
Close to Pin 34,35,36



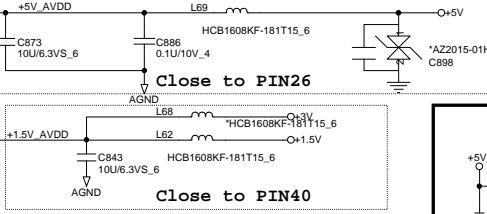
Close to Pin 41



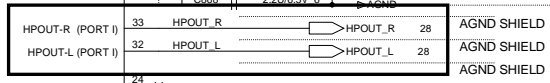
Close to Pin 46



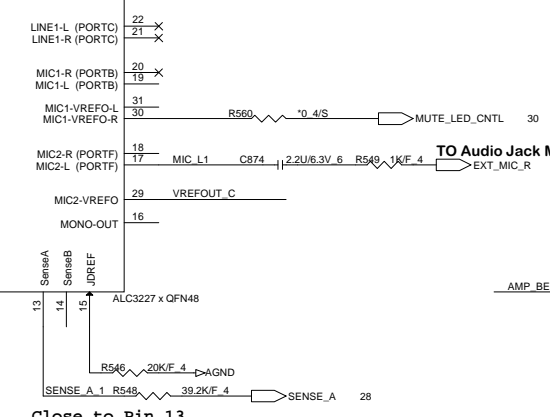
>40mils trace



Analog



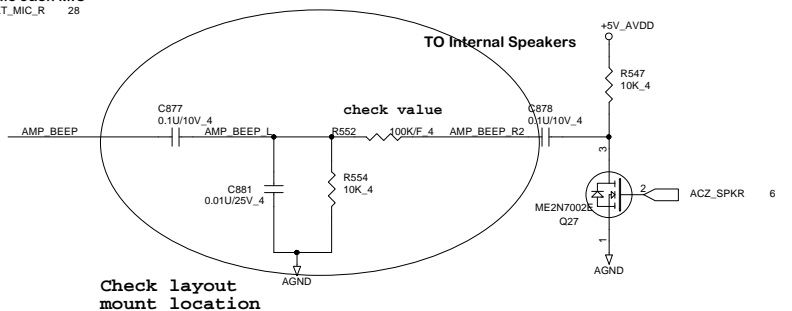
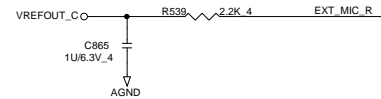
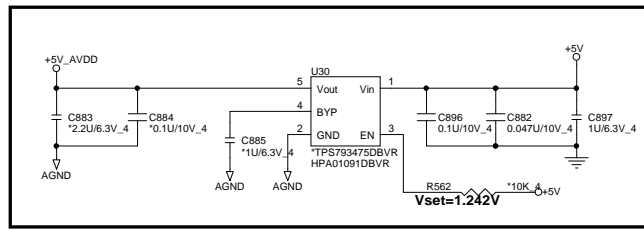
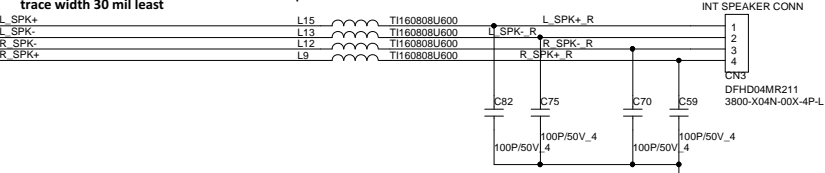
DB swap HPOUT_R/L



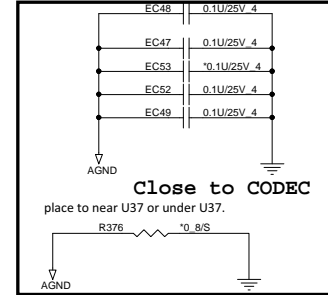
Close to Pin 13



Close to CODEC



Check layout mount location

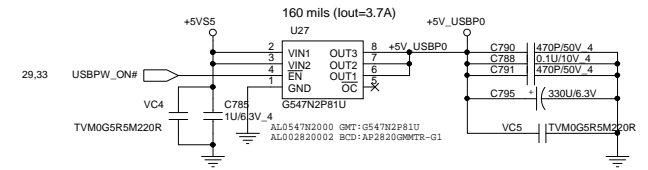
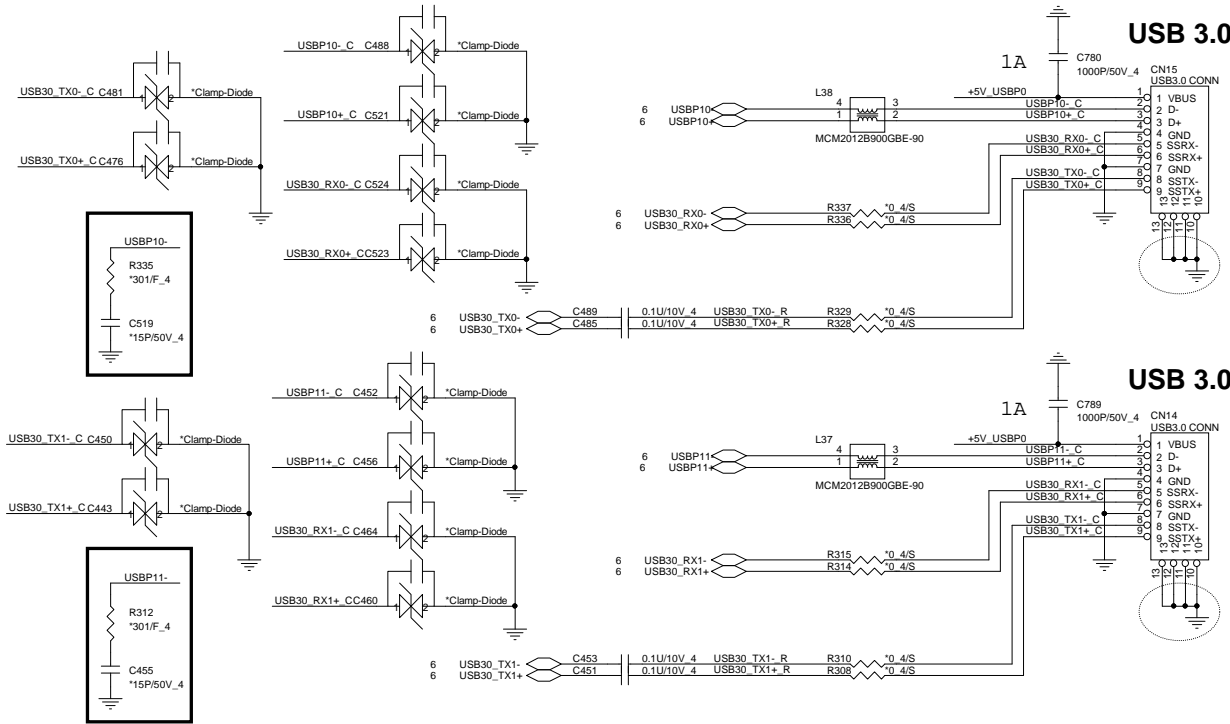


PROJECT : R7X
Quanta Computer Inc.

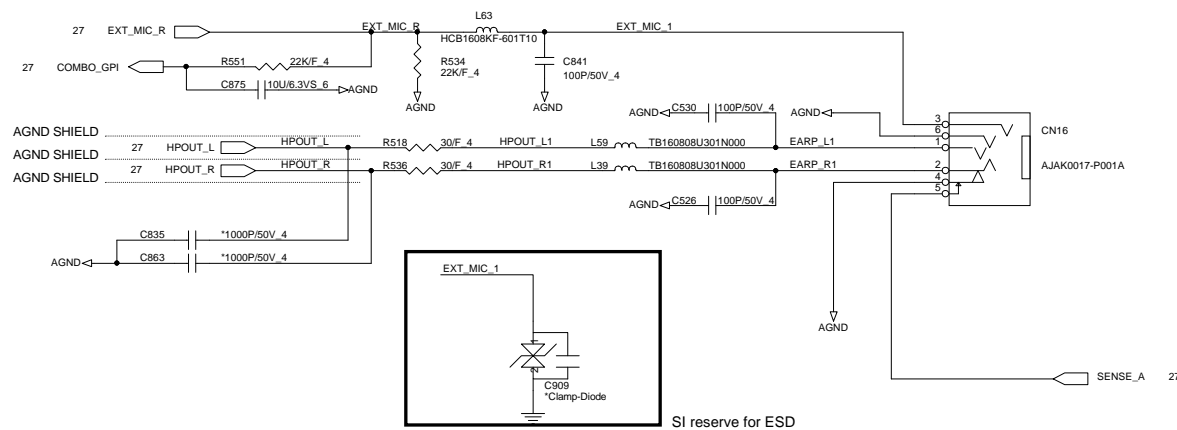
Size: Custom
 Document Number: Azalia ALC3227
 Date: Tuesday, March 12, 2013
 Sheet: 27 of 43


NB5

USB3.0 X 2/USB2.0 COMBO



COMBO JACK



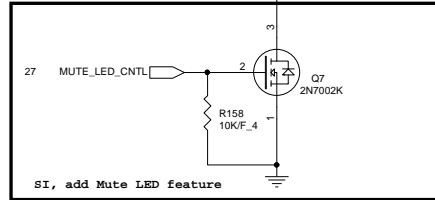
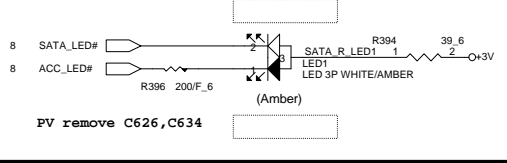
 PROJECT : R7X Quanta Computer Inc.	
Size Custom	Document Number USB/Audio Jack
Date: Tuesday, March 12, 2013	Sheet 28 of 43



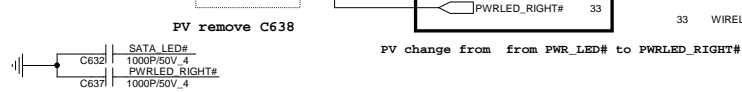
KEYBOARD Con.



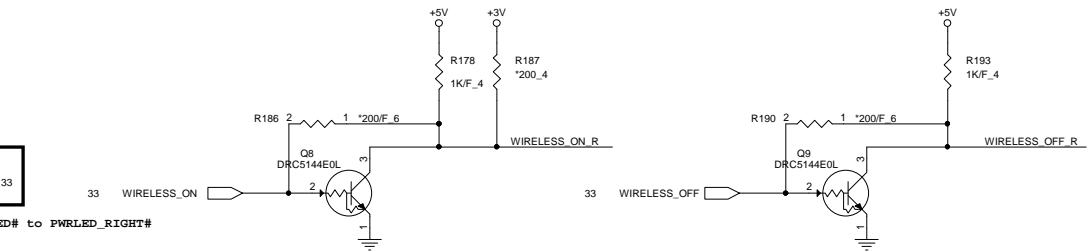
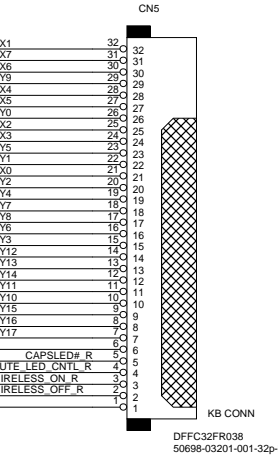
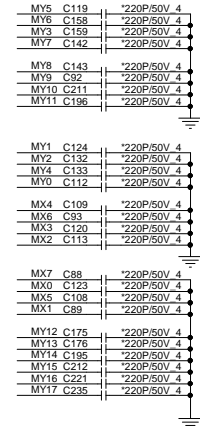
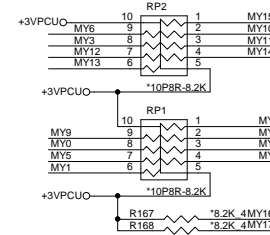
SATA_LED



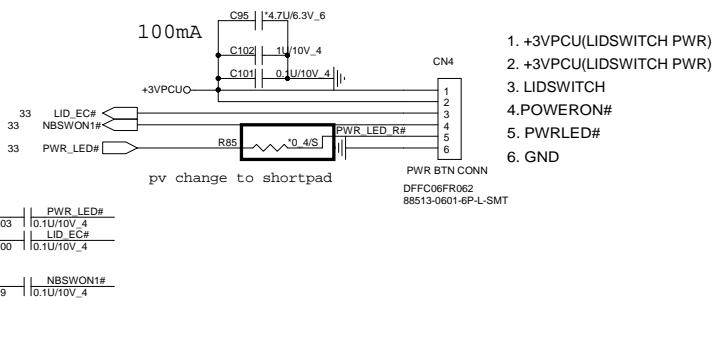
PWR_LED



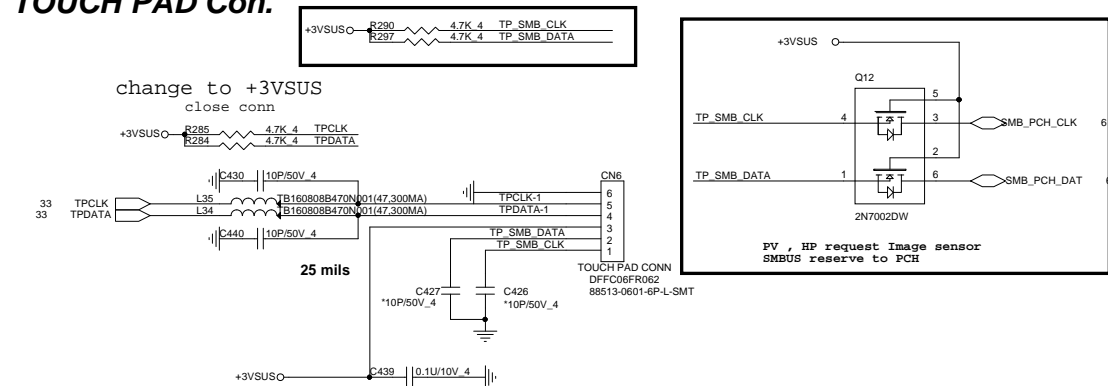
KEYBOARD PULL-UP



POWER BOTTON CONNECT



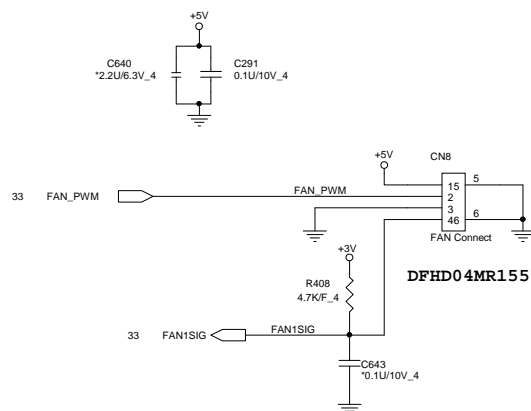
TOUCH PAD Con.



PROJECT : R7X
Quanta Computer Inc.

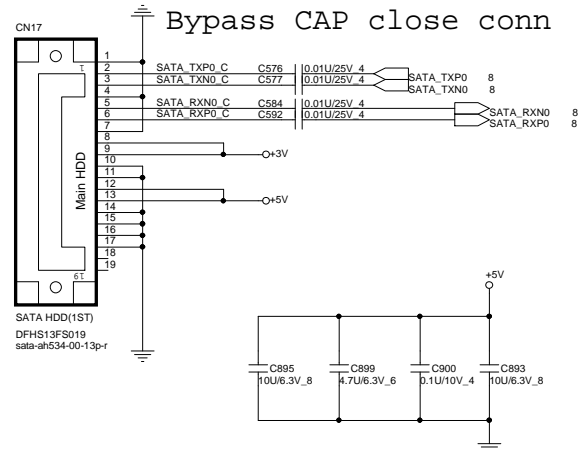
Size Custom	Document Number LED/KB/SW/TP	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 30 of 43	

CPU FAN

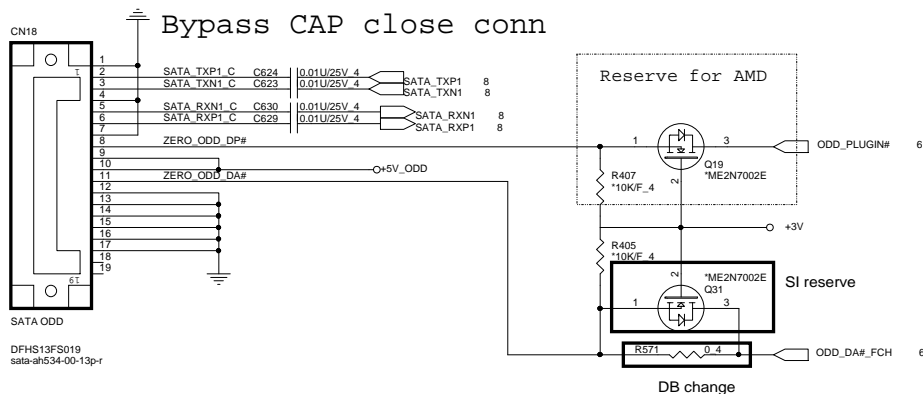


SATA HDD CONNECTOR

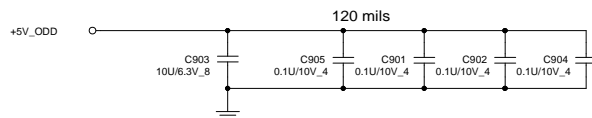
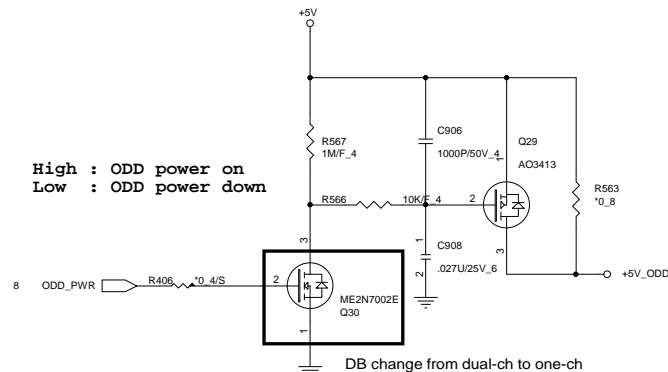
31



SATA ODD CONNECTOR



High : ODD power on
Low : ODD power down



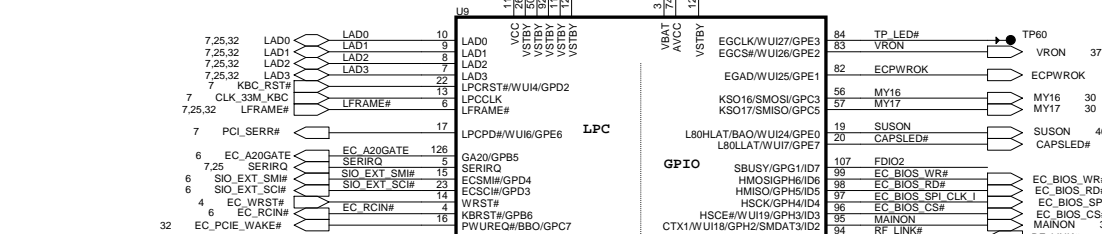
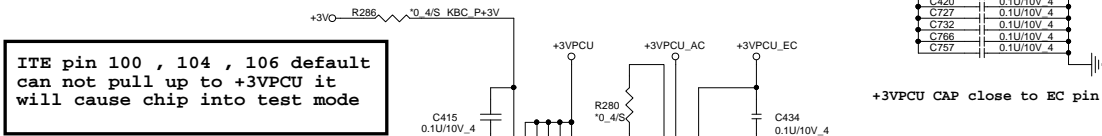
		PROJECT : R7X Quanta Computer Inc.	
Size	Custom	Document Number	Rev
		HDD/ODD/FAN	1A
Date:	Tuesday, March 12, 2013	Sheet	31 of 43

2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,33,41,42,43
2,4,22,23,27,38,41
7,25,30,33,34,35
8,24,25,26,27,30,31,41
+1.5V
+3V
+3VPCU
+5V

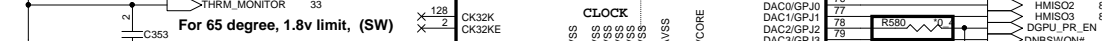
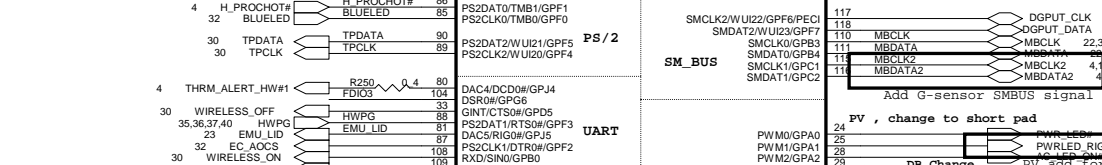
2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,32,41,42,43
7,25,30,32,34,35
34,35,36



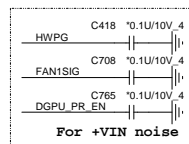
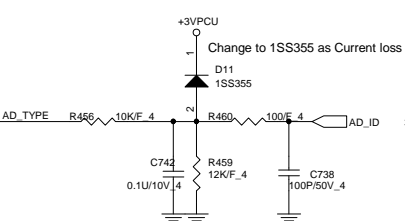
ITE pin 100 , 104 , 106 default
can not pull up to +3VPCU it
will cause chip into test mode



IT8528E/HX

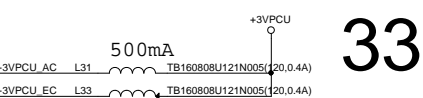
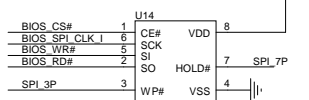


Smart adapter Type check

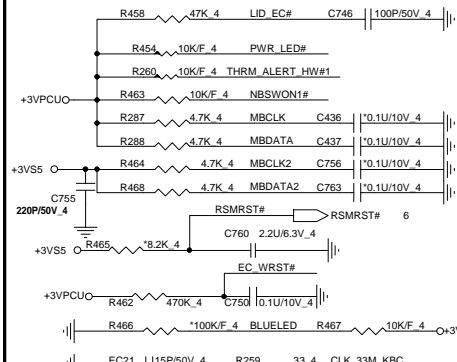
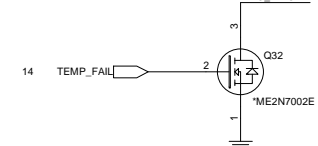


Vender	Size	P/N
AMIC	4M	AKE39ZN0800
EON	4M	AKE39ZN0Q03
WINBOND	4M	AKE39FN0N01
Socket		DFHS08FS023

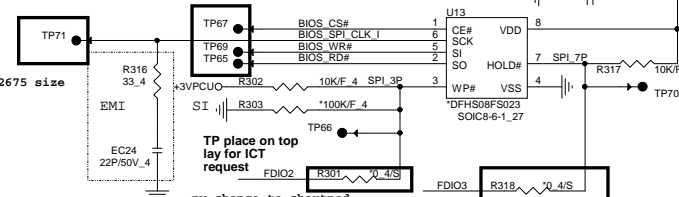
4M SPI EC ROM



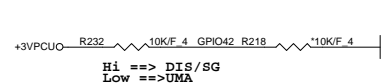
DGPU Thermal protect



128K byte SPI EC ROM



Adapter select

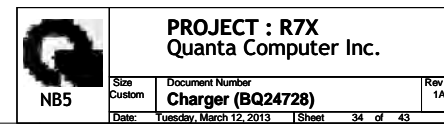


Platform model	GPI042	adapter
SG/DIS	High	90W
UMA	Low	65W

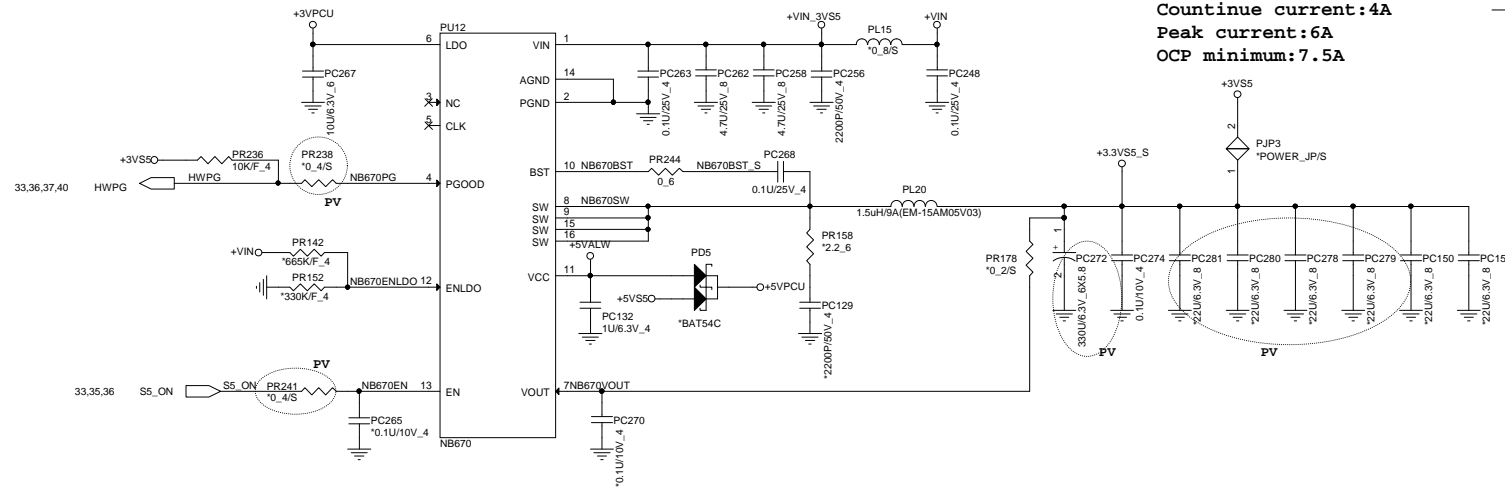


PROJECT : R7X
Quanta Computer Inc.

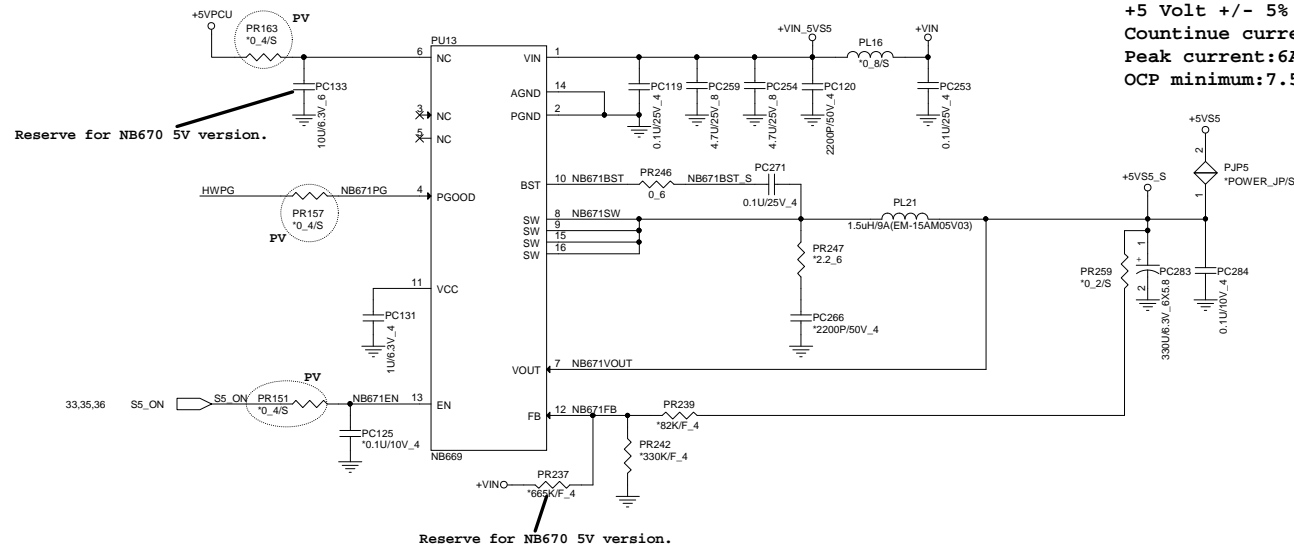
Size	Document Number	Rev
Custom	EC (IT8518E/HX)ROM	1A
Date: Tuesday, March 12, 2013	Sheet 33 of 43	



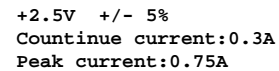
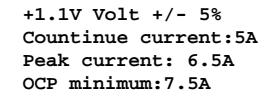
+3.3 Volt +/- 5%
Continue current:4A
Peak current:6A
OCP minimum:7.5A



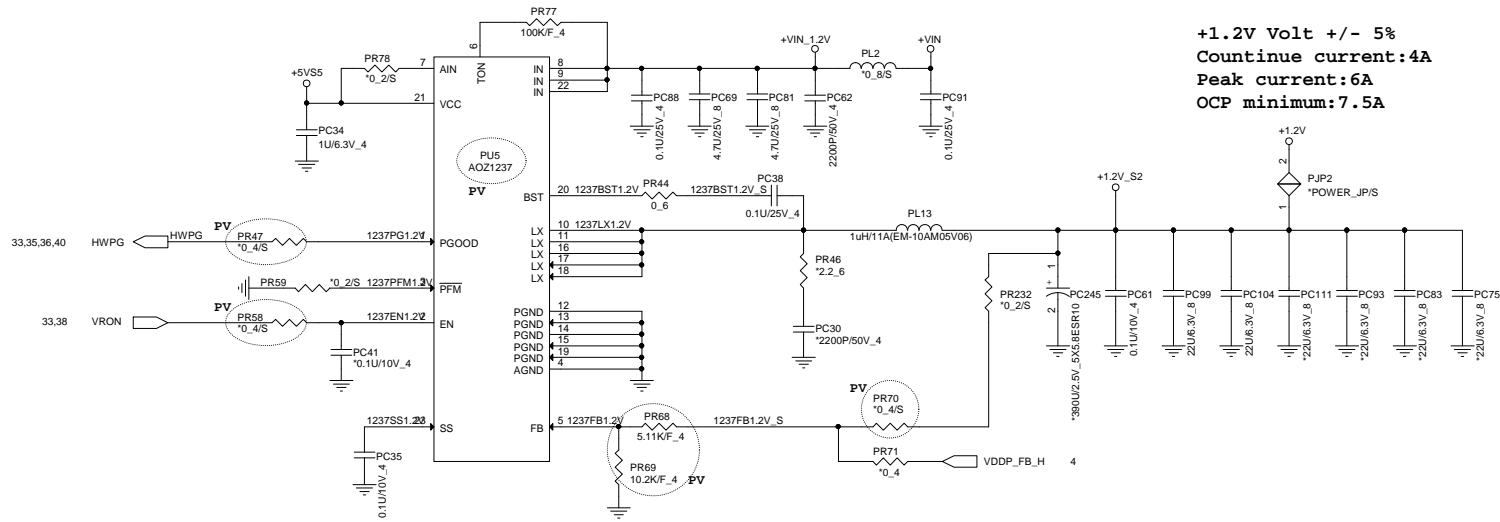
+5 Volt +/- 5%
Continue current:4A
Peak current:6A
OCP minimum:7.5A

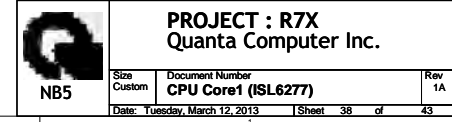


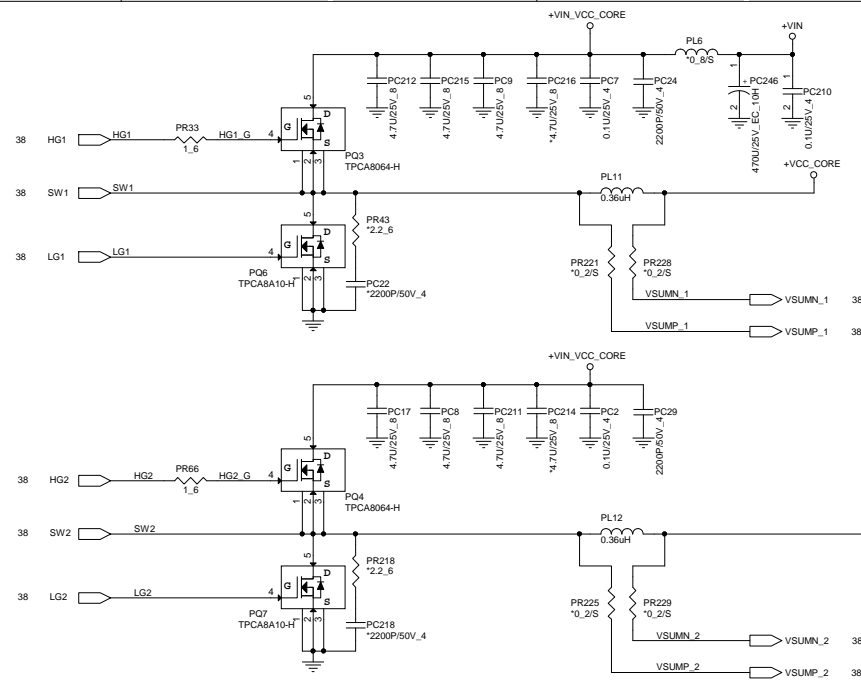
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Size Custom	Document Number +1.1VS5 (AOZ1237)/2.5V	Rev 1A
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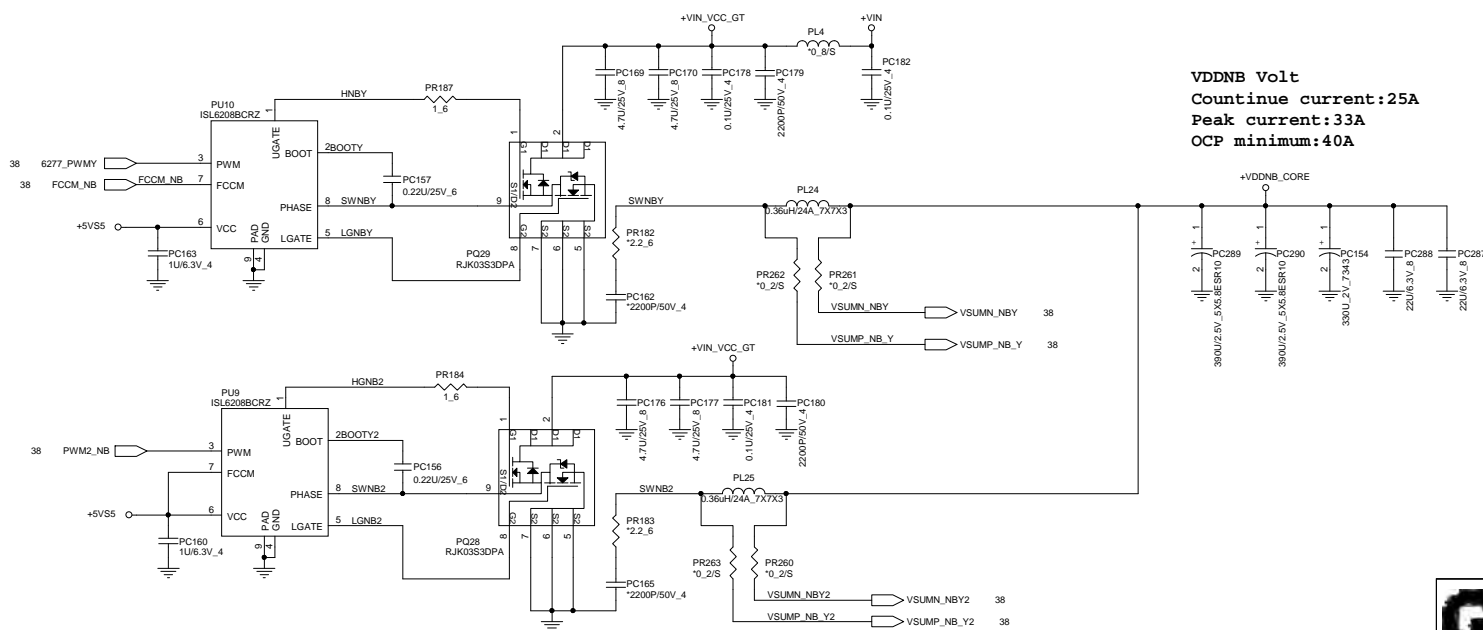





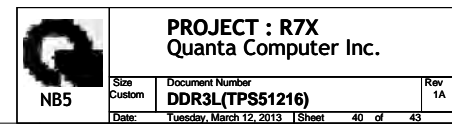


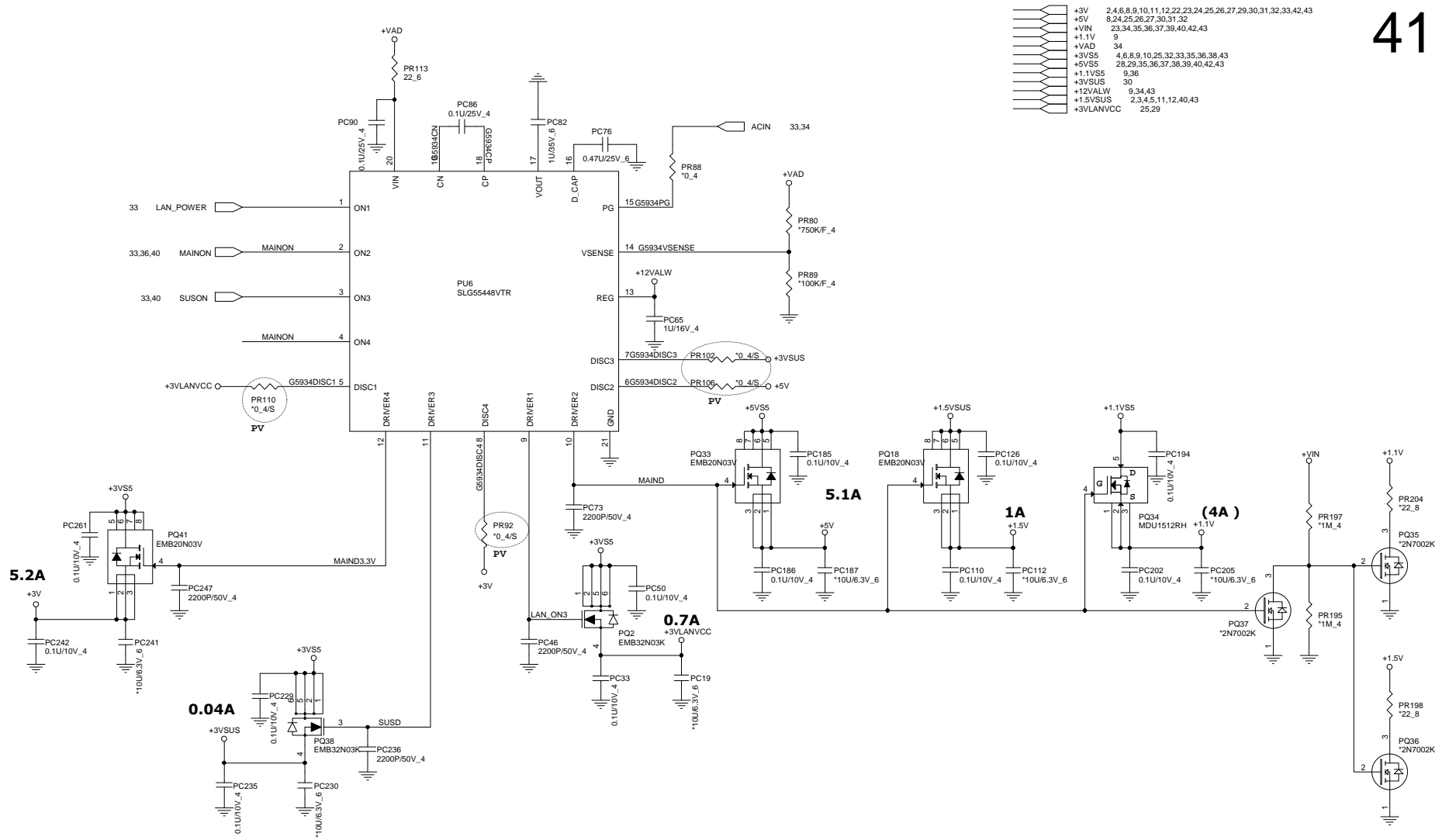
CPU CORE Volt
 Countinue current:36A
 Peak current:50A
 OCP minimum:60A

VDDNB Volt
 Countinue current:25A
 Peak current:33A
 OCP minimum:40A



 <p>NB5</p>	<p>PROJECT : R7X Quanta Computer Inc.</p>		
	<p>Size Custom</p>	<p>Document Number CPU Core2 (ISL6208)</p>	<p>Rev 1A</p>
	<p>Date: Tuesday, March 12, 2013 Sheet 39 of 43</p>		





VGA Core

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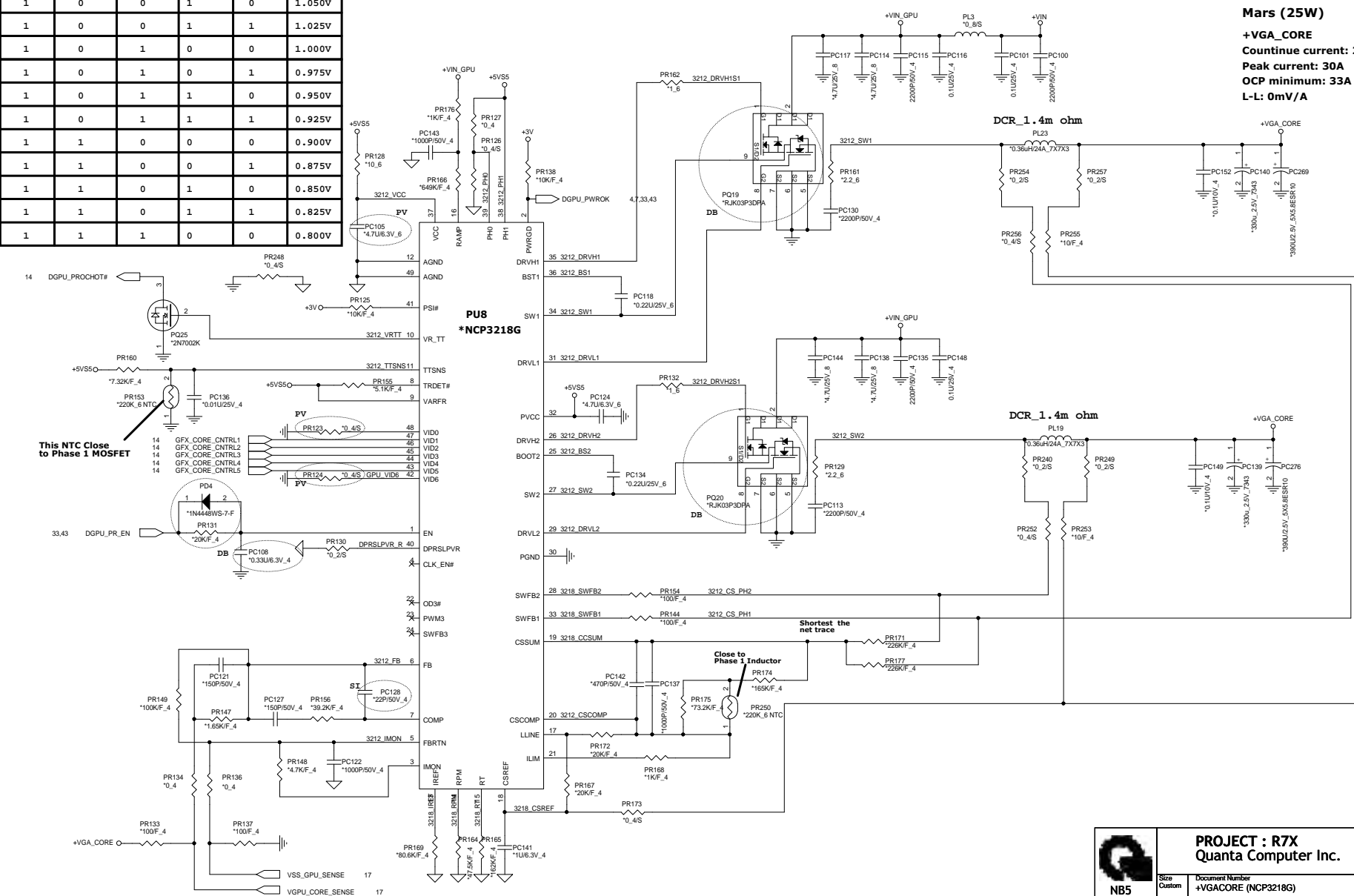
+VGA_CORE 17.43

Mars (25W)

+VGA_CORE
Continue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L: 0mV/A

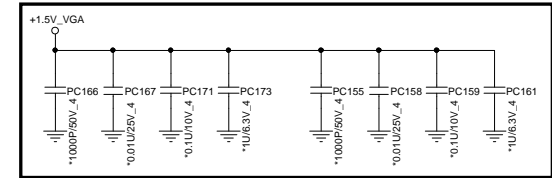
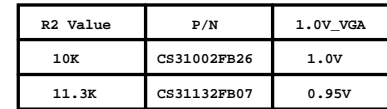
GPIO10	GPIO12	GPIO16	GPIO20	GPIO15	Mars XT
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

Default



PROJECT : R7X
Quantia Computer Inc.

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